37.4.309 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR17)

Address: 20E_0000h base + 4E4h offset = 20E_04E4h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															HYS
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PUS		PUE	PKE	ODE	0			SPEED		DSE			0		SRE
W																
Reset	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0	1

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR17 field descriptions

Field	Description
31–17 Reserved	This read-only field is reserved and always has the value 0.
16 HYS	Hysteresis Enable Field Select one of next values for pad: EIM_A17. 0 **DISABLED** — CMOS input 1 **ENABLED** — Schmitt trigger input
15–14 PUS	Pull Up / Down Config. Field Select one of next values for pad: EIM_A17. 00 **100K_OHM_PD** — 100K Ohm Pull Down 01 **47K_OHM_PU** — 47K Ohm Pull Up 10 **100K_OHM_PU** — 100K Ohm Pull Up 11 **22K_OHM_PU** — 22K Ohm Pull Up
13 PUE	Pull / Keep Select Field Select one of next values for pad: EIM_A17. 0 **KEEP** — Keeper Enabled 1 **PULL** — Pull Enabled
12 PKE	Pull / Keep Enable Field Select one of next values for pad: EIM_A17. 0 **DISABLED** — Pull/Keeper Disabled 1 **ENABLED** — Pull/Keeper Enabled
11 ODE	Open Drain Enable Field Enables open drain of the pin. 0 **DISABLED** — Output is CMOS. 1 **ENABLED** — Output is Open Drain.

Table continues on the next page...

IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR17 field descriptions (continued)

Field	Description
10–8 Reserved	This read-only field is reserved and always has the value 0.
7–6 SPEED	Speed Field Select one of next values for pad: EIM_A17. 00 **RESERVED0** — Reserved 01 **50MHZ** — Low (50 MHz) 10 **100MHZ** — Medium (100 MHz) 11 **200MHZ** — Maximum (200 MHz)
5–3 DSE	Drive Strength Field Select one of next values for pad: EIM_A17. 000 **HIZ** — HI-Z 001 **240_OHM** — 240 Ohm 010 **120_OHM** — 120 Ohm 011 **80_OHM** — 80 Ohm 100 **60_OHM** — 60 Ohm 101 **48_OHM** — 48 Ohm 110 **40_OHM** — 40 Ohm 111 **34_OHM** — 34 Ohm
2–1 Reserved	This read-only field is reserved and always has the value 0.
0 SRE	Slew Rate Field Slew rate control. 0 **SLOW** — Slow Slew Rate 1 **FAST** — Fast Slew Rate

37.4.310 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_EIM_ADDR18)

Address: 20E_0000h base + 4E8h offset = 20E_04E8h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															HYS
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PUS		PUE	PKE	ODE	0			SPEED		DSE			0		SRE
W																
Reset	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0	1