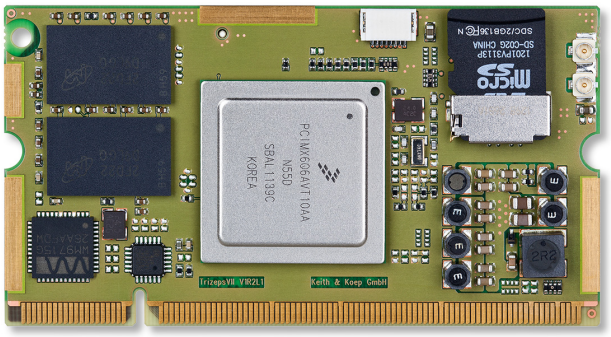
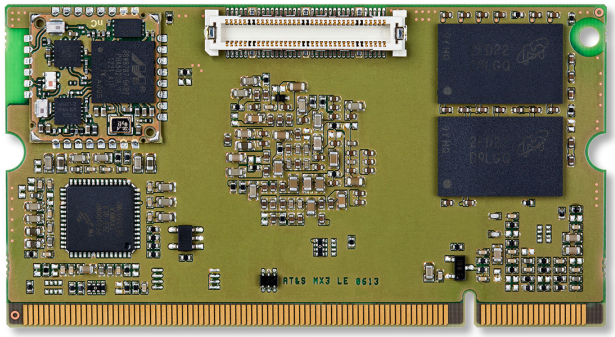
TrizepsVII_V1R2 - Datasheet 2.0.9 (Preliminary)





1.0 Introduction

The Trizeps VII module is powered by the Freescale™ i.MX 6 series scalable multicore platform that includes a single-, dual- and quad-core processor. The ARM® Cortex™-A9 cores clock up to 1.0 GHz, featuring the ARMv7™ instruction set, Neon general-purpose SIMD engine, the VFPv3 floating-point architecture, and support for ARM®'s TrustZone secure computing technology.
The ARM® Cortex™-A9 architecture supports power-efficient processing capabilities with 512 KB up to 1 MB L2 cache and scalability of 512 MB up to 2 GB 64-Bit DDR3-1066 memory. For high multimedia level performance tasks the 3D Vivante GC2000 GPU and 2D Vivante GC3500 GPU graphics are integrated and support multi-stream-capable high-definition video encoding, decoding as well as 3D video playback. A performance of 200 MT/s with up to quad shaders is reached by the 3D graphic engine and the additional separate 2D Vertex acceleration engine is used for an optimal user interface experience with rich GUIs.
Integrated comprehensive market-specific IOs in the i.MX 6 series are used in the Trizeps VII to be fully compatible to previous Trizeps Modules and enhance with a 60pol new high-speed board to board connector additional multimedia interfaces to the standard platform. For default peripherals, the CPU module has beside the integrated PHYs an onboard 10/100 Mbit Ethernet PHY, an AC'97 Audio and Touchpanel codec, and a radio module for WLAN and Bluetooth.

Main features of Trizeps-VII

Feature	Description	Options available on Trizeps VII
Processor	Freescale™ i.MX 6 ARM® Cortex™ A9, MP-CPU, 800MHz up to 1.0 GHz per Core, 1 MB L2 Cache	CPU-Type: Quad (Q), Dual (D), DualLite (U) and Solo (S)
Memory	1,2,4 x 16 Bit DDR3-1066 (533 MHz), 1 CS @Q&D 1,2,4 x 16 Bit DDR3-800 (400 MHz), 1 CS @U 1,2 x 16 Bit DDR3-800 (400 MHz), 1 CS @S	Total RAM Memory available: 1 GB @Q&D, 512 MB @U&S, 2 GB and 256MB on request
Storage	onBoard 8 Bit wide eMMC or 4 Bit wide µSD Socket	eMMC 4 GB (Option up to 64 GB), µSD 4 GB (Option up to 32 GB)
Radio	onBoard WLAN-Bluetooth module, fits four different module types	IEEE 802.11 a/b/g/n/e/i/h/d/k/r/w, 72 Mbps (20 MHz) and up to 150 Mbps (40 MHz), Bluetooth 3.0+ EDR

onBoard features (included without any options)

Display interfaces: (supports 3D, 4k x 2k and 2x 1080p Displays) HDMI v1.4, 2x LVDS, LCD 24 RGB, MIPI serial Display

Camera interfaces: (supports 2x cameras at the same time) 8bit parallel camera and MIPI serial camera

Ethernet: onBoard 10/100Mbit RMII PHY and 10/100/1000Mbit RGMII interface (only one interface useable at the same time)

Power: High-Eff. PMIC with single +3V3 supply (below 3-5W), controlled by I2C

Interfaces: USB2.0 Host and OTG, 2x FlexCAN, S-ATA II, PCIe, RTC, SPDIF, Adress-Data-Bus, 3x UARTs, 2x I2C, 2x SPI, GPIOs, 2x PWMs,

Audio Codec: AC'97 Audio Codec with 4/5 wires res. Touch and 4x 12bit ADC (2x comparator inputs for battery monitoring)

Extension Connector: additional FX11 60pol. high-speed board to board connector, mechanical compatibility warranted

SODIMM200 card edge connector: pin compatible to all Keith & Koep Trizeps IV, IV-M, IV-WL, V and VI Modules

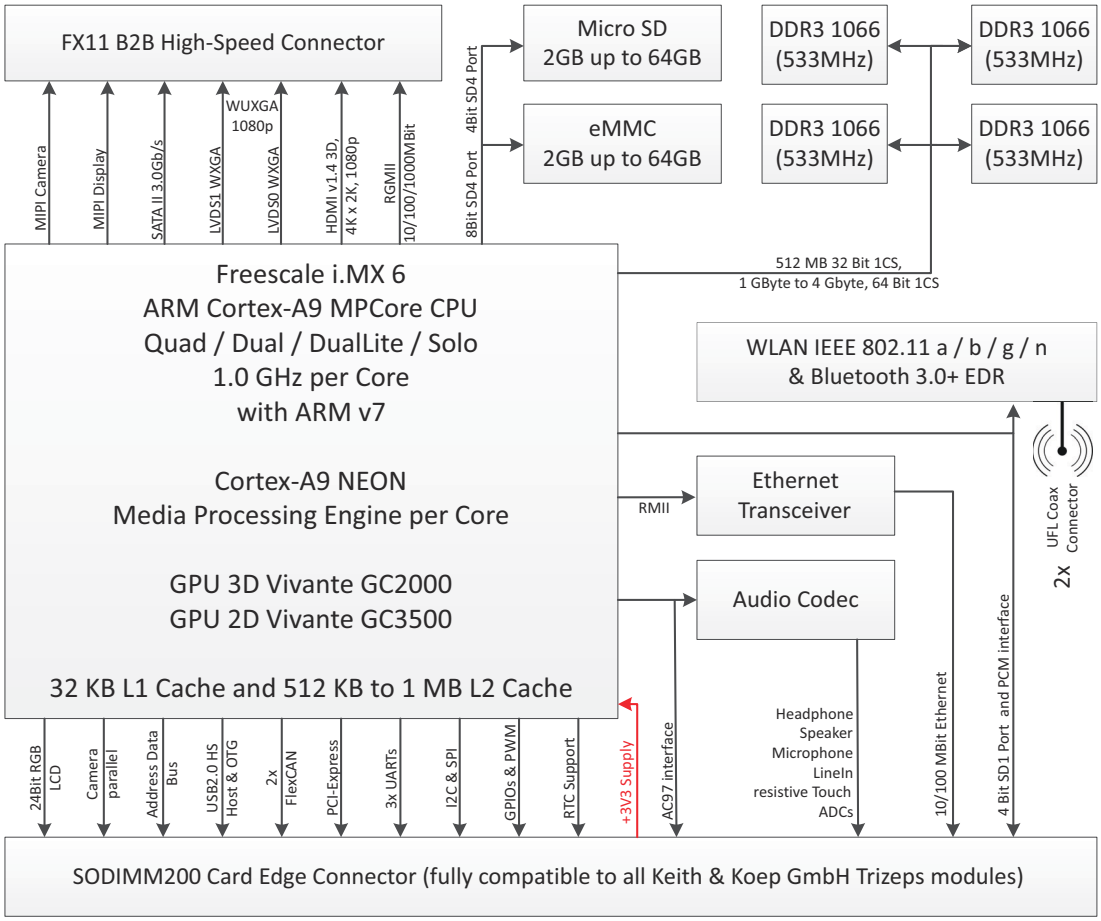
2.0 Functional description of the Trizeps-VII Module

In the following you'll find special information about the Trizeps VII Module. For more information concerning the Freescale, Wolfson, SMSC, Lesswire peripherals please refer to the manufacturers original manuals:

i.MX 6 http://www.freescale.com
WM9715 http://www.wolfsonmicro.com
LAN8720A http://www.smsc.com
WiBear11n http://www.lesswire.com

For more details about the Trizeps VII, please also see the documentation at
http://www.keith-koep.com/service/doku.php/de/service

Figure 1. Trizeps-VII Module Block diagram



Main components of the Trizeps-VII Module:

1. Freescale i.MX 6 Quad (Q) / Dual (D) / DualLite (U) / Solo (S) (microprocessor)
2. WM9715 (a single chip, stereo Audio Codec equipped with Touch screen and power management interfaces)
3. 4 x 16 Bit DDR3-1066 (533 MHz) or DDR3-800 (400 MHz), 64-Bit 1 CS
4. eMMC 8-Bit wide or µSD Socket 4-Bit wide
5. LAN8720A RMII 10/100 Ethernet Transceiver with HP Auto-MDIX Support
6. PMIC with I2C management interface
7. FX11 60pol. board to board high-speed connector
8. 802.11 a/b/g/n WLAN and Bluetooth 3.0+ EDR radio module

2.1 Interfaces of the i.MX 6 on SODIMM200 socket

The Trizeps-VII Module offers the following interfaces:

2.1.1 Universal Asynchronous Receiver / Transmitter (UART) serial ports

Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility. UART supports NRZ encoding format , RS485 compatible 9 bit data format and IrDA-compatible infrared slow data rate (SIR) format.

The UART includes the following features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9 bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- RS-485 driver direction control via CTS signal
- Edge-selectable RTS and edge-detect interrupts
- Status flags for various flow control and FIFO states
- Voting logic for improved noise immunity (16x oversampling)
- Transmitter FIFO empty interrupt suppression
- UART internal clocks enable/disable
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RXD input and TXD output can be inverted respectively in RS-232/RS-485 mode
- DCE/DTE capability
- RTS, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE),
- RI (DTE only), DCD (DTE only), DTR (DCE only) and DSR (DTE only) interrupts wake the processor from STOP mode
- Maskable interrupts
- Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
- Escape character sequence detection
- Software reset (SRST)
- Two independent, 32-entry FIFOs for transmit and receive
- The peripheral clock can be totally asynchronous with the module clock. The module clock determines baud rate. This allows frequency scaling on peripheral clock (such as during DVFS mode) while remaining the module clock frequency and baud rate.

Accessible on SODIMM200 socket:

UART1: TxD, RxD, CTS and RTS (with boot messages)

Additional GPIOs for Full-Function-UART:

RI (GPIO1_5), DCD (GPIO6_15), DSR (GPIO6_14), DTR (GPIO7_7)

UART2: TxD, RxD, CTS and RTS

UART4: TxD and RxD

2.1.2 Universal Serial Bus (USB) Host and OTG-Controller

The USB controller block provides high performance USB functionality that conforms to the USB 2.0 specification, and the OTG supplement.

Two integrated USB 2.0 PHY macrocells capable of connecting to USB host/device systems at the USB low-speed (LS) rate of 1.5 Mbits/s, full-speed (FS) rate of 12 Mbits/s or at the USB 2.0 high-speed (HS) rate of 480 Mbits/s.

The integrated PHY provides a standard UTM interface. The USB_DP and USB_DN pins connect directly to a USB connector. USBPHY1 is the PHY interface for USB OTG controller; USBPHY2 is the PHY interface for USB Host1 controller.

Accessible on SODIMM200 socket:

USB2.0 Host: DP, DN, PEN, OC

USB2.0 OTG: DP, DN, PEN, OC, ID, VBUS, \CHD (Charge Detect for LED),
Slave plug detect from previous Trizeps modules: IRQ_SLAVE_CD (GPIO2_5)

2.1.3 I2C Bus Interface Unit

The Inter IC interface provides functionality of a standard I2C slave and master. The I2C is designed to be compatible with the standard Philips I2C bus protocol. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This Bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C interface operates up to 400 kbps, but it depends on the pin loading and timing characteristics. For pin requirement details, refer to Philips I2C Bus Specification, Version 2.1. The I2C system is a true multiple-master bus including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.

The I2C includes the following features:

- Compatibility with I2C bus standard
- Multiple-master operation
- Software-programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

Accessible on SODIMM200 socket:

I2C_1: I2C1_SCL, I2C1_SDA (also possible to support DDC protocol for HDMI1.4)

I2C_2: I2C2_SCL, I2C2_SDA (communication with PMIC and EEPROM)

DDC for HDMI: DDC_SDA Pin149, DDC_SCL Pin130

Freescale claims to connect maximal four I2C devices on one I2C bus.

Please also refere to „20130526_AN_TrizepsVII_V1R2_I2CAddress.pdf“ to avoid address conflicts.

2.1.4 Ultra Secured Digital Host Controller (uSDHC)

The Ultra Secured Digital Host Controller provides the interface between the host system and the SD/SDIO/MMC cards. The uSDHC acts as a bridge, passing host bus transactions to the SD/SDIO/MMC cards by sending commands and performing data accesses to/from the cards. It handles the SD/SDIO/MMC protocols at the transmission level. Different types of cards supported by the uSDHC are described briefly as follows: The Multi Media Card (MMC) is a universal low cost data storage and communication media that is designed to cover a wide area of applications including mobile video and gaming. Old MMC cards are based on a 7-pin serial bus with a single data pin, while the new high speed MMC communication is based on an advanced 11-pin serial bus designed to operate in the low voltage range.The Secure Digital Card (SD) is an evolution of the old MMC technology. It is specifically designed to meet the security, capacity, performance, and environment requirements inherent in newly emerging audio and video consumer electronic devices. The physical form factor, pin assignment and data transfer protocol are forward compatible with the old MMC (with some additions). Under the SD protocol, it can be categorized into Memory card, I/O card and Combo card, which has both memory and I/O functions. The memory card invokes a copyright protection mechanism that complies with the security of the SDMI standard. The I/O card, which is also known as SDIO card, provides high-speed data I/O with low power consumption for mobile electronic devices. For the sake of simplicity, the following figure does not show cards with reduced size or mini cards.

The features of the uSDHC module include the following:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4
- Compatible with the SD Memory Card Specification ver. 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification ver. 3.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 208 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modesdevices
- Up to 200 Mbps of data transfer for SDIO cards using 4 parallel data lines
- Up to 832 Mbps of data transfer for SDXC cards using 4 parallel data lines in SDR(Single Data Rate) mode
- Up to 400 Mbps of data transfer for SDXC card using 4 parallel data lines in DDR(Dual Data Rate) mode
- Up to 416 Mbps of data transfer for MMC cards using 8 parallel data lines in SDR(Single Data Rate) mode
- Up to 832 Mbps of data transfer for MMC cards using 8 parallel data lines in DDR(Dual Data Rate) mode
- Supports Single Block, Multi Block read and write
- Supports block sizes of 1 ~ 4096 bytes
- Supports the write protection switch for write operations
- Supports both synchronous and asynchronous abort
- Supports pause during the data transfer at block gap
- Supports SDIO Read Wait and Suspend Resume operations
- Supports Auto CMD12 for multi-block transfer
- Host can initiate non-data transfer command while data transfer is in progress
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes, also supports interrupt period
- Embodies a fully configurable 128x32-bit FIFO for read/write data
- Supports internal and external DMA capabilities
- Support voltage selection by configuring vendor specific register bit
- Supports Advanced DMA to perform linked memory access

Accessible on SODIMM200 socket:

SD1: SDIO interface to WiBear WLAN Bluetooth Module or assembly option for second SODIMM200 interface

SD2: first SDIO interface on SODIMM200

SD4: 8 Bit wide eMMC or 4 Bit wide µSD Card Socket on TrizepsVII

2.1.5 10/100Mbit Ethernet

The Trizeps VII module contains a high performance single-Chip RMII 10/100Mbit Ethernet Physical Layer Transceiver (PHY) with HP Auto-MDIX Support with flexible power management architecture to optimize system power consumption.

The features of the Ethernet PHY include the following:

- Compliant with IEEE802.3/802.3u (Fast Ethernet)
- Compliant with ISO 802-3/IEEE 802.3 (10BASE-T)
- Loop-back modes
- Auto-negotiation
- Automatic polarity detection and correction
- Link status change wake-up detection
- Vendor specific register functions
- Supports the reduced pin count RMII interface

Accessible on SODIMM200 socket:

Transmit: ENET1 TXP, TXN

Receive: ENET1 RXP, RXN

LEDs: ENET1 \LINK_AKT, ENET1 \SPEED

2.1.6 Enhanced Configurable SPI (ECSPI)

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block. The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). With data FIFOs, the ECSPI allows rapid data communication with fewer software interrupts.

Key features of the ECSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency.

Accessible on SODIMM200 socket:

SPI1 SS 0 + MOSI + MISO + SCLK:
assembly option with parallel camera interface CSIO: VSYNC, HSYNC, MCLK, PCLK

SPI5 SS 0-2 + MOSI + MISO + SCLK:
muxed with WLAN SD1 and is an assembly option of Display Data 18-23
SS 3 is muxed with SD2 Data 3

2.1.7 GPIO

The GPIO general-purpose input / output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts. The GPIO is one of the blocks controlling the IOMUX of the Chip.

The GPIO includes the following features:

- General purpose input/output logic capabilities:
- Drives specific data to output using the data register (GPIO_DR)
- Controls the direction of the signal using the GPIO direction register (GPIO_GDR)
- Enables the core to sample the status of the corresponding inputs by reading the pad sample register (GPIO_PSR).
- GPIO interrupt capabilities:
- Supports up to 32 interrupts
- Identifies interrupt edges
- Generates three active-high interrupts to the SoC interrupt controller

Accessible on SODIMM200 socket:

GPIO1_5	(UART1_RI)
GPIO2_3	general GPIO
GPIO2_4	general GPIO
GPIO2_5	(IRQ_USB_SLAVE_CD)
GPIO2_27	general GPIO
GPIO5_28	general GPIO
GPIO5_29	(EIM_RD/RW)
GPIO6_9	(general GPIO)
GPIO6_15	(UART1_DCD)
GPIO6_14	(UART1_DSR)
GPIO7_7	(UART1_DTR)

Special Function Pins on SODIMM200 socket:

IRQ	(special interrupt GPIO, but all Trizeps VII GPIOs are interrupt capable)
\RESET_IN	(force i.MX 6 to reset)
\RESET_OUT	(resets external peripherals)
VDD_OTP	(only for internal use!)
+1V8	(for low current applications)
RTC_LICELL	(connect LiPo, 3V Battery or +3V3 for internal RTC support)

Please also refere to „sodimm200_standard_v7.xls“, which lists PinMUX options and reset conditions.

2.1.8 Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) has a 16-bit counter, and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4 x 16 data FIFO.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

Accessible on SODIMM200 socket:

PWM1	general PWM
PWM2	(Display BL PWM)

2.1.9 Codec Wolfson WM9715

The WM9715L is a highly integrated input / output device which connects directly to a 4-wire or 5-wire touchpanel, mono or stereo microphones, stereo headphones and a mono speaker.The Codec also offers up to four auxiliary ADC inputs for analogue measurements such as temperature or light. To monitor the battery voltage in portable systems, the WM9715L has two uncommitted comparator inputs. All device functions are accessed and controlled through a single AC-Link interface compatible with the AC'97 standard(rev 2.2). Additionally, the WM9715L can generate interrupts to indicate pen down, pen up, availability of touchpanel data, low battery, and dead battery.

The features of the Codec include the following:

- Microphone mono input with Automatic Level Control (ALC)
- LineIn stereo input
- Headphone stereo output 16R / 32R 45mW
- Speaker mono output 8R 400mW
- 4x 12Bit auxiliary ADCs inputs (2 comparator inputs for battery monitoring)
- 4/5 wires resistive Touch
- 12-bit resolution, INL LSBs (<0.5 pixels)
- X, Y and touch-pressure (Z) measurement
- Pen-down detection supported in Sleep Mode
- external Audio Power Input +3V3 for LDO

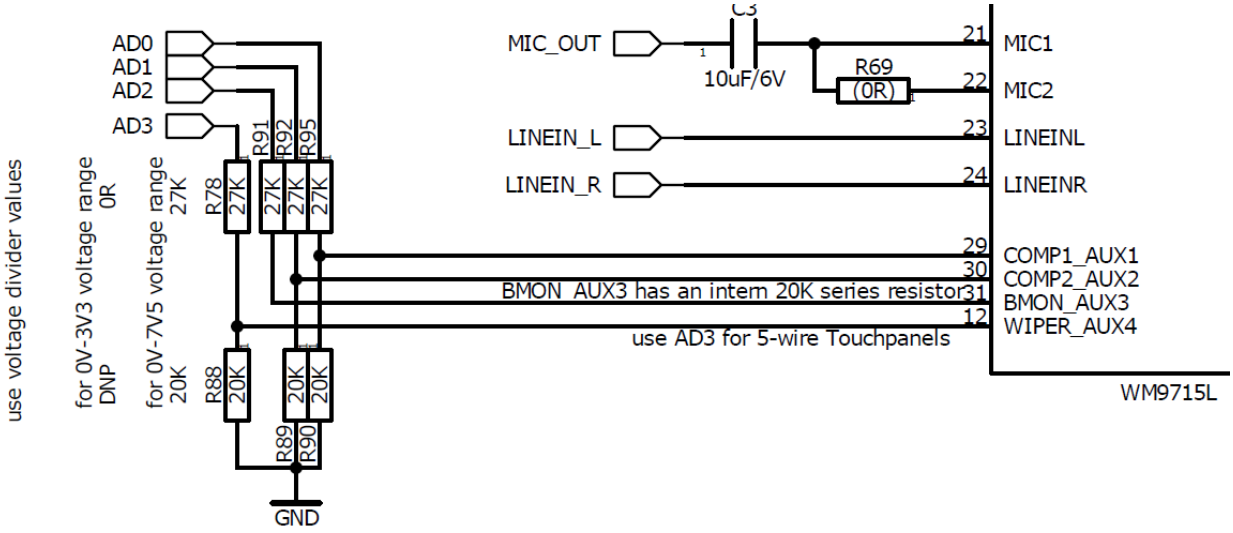
Accessible on SODIMM200 socket:

Input: Microphone (mono), LineIn (stereo), 4x ADCs, 4x res. Touch, +3V3 Audio LDO

Output: Headphone (stereo), Speaker (mono)

Standard ADC input range: 0V - 3V3. With additional voltage divider on TrizepsVII pcb: 0V - 7V5. (see Figure 2)

Figure 2. ADC-wiring



2.1.10 Sony/Philips Digital Interface (SPDIF)

The Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF transceiver allows the handling of both SPDIF channel status (CS) and User (U) data and includes a frequency measurement block that allows the precise measurement of an incoming sampling frequency. A recovered clock is provided to drive both internal and external components in the system such as ESAI ports, as well as external A/Ds or D/As, with clocking control provided via related registers. As the SPDIF internal data width is 24-bit, the eight most-significant bits of all registers return zeros.

Accessible on SODIMM200 socket:

Input: SPDIF IN(muxed with EIM_D21)

Output: SPDIF OUT(muxed with EIM_D22)

2.1.11 JTAG / Debug Port

The System JTAG Controller (SJC) provides debug and test control with the maximum security. The test access port (TAP) is designed to support features compatible with the IEEE Standard 1149.1 v2001 (JTAG). IEEE P1149.6 standard extensions for AC testing is provided for selected analog IO pads of PCIe and SATA modules.
The JTAG / Debug port consists of several shift registers, with the destination controlled by the TMS pin and data I/O with TDI / TDO. The Debug Port is accessible through an additional FFC 8pol. connector with an Keith & Koep specific adapter pcb. For detailed information please contact Keith & Koep GmbH.

The JTAG / Debug port provides two different functionalities:

- Programming Flash memory (eMMC or µSD) by pushing data through the shift registers
- Hardware-testing using boundary scan interface according to IEEE 1149.1

2.1.12 PCI Express

PCIe 2.0 PHY is a complete mixed-signal semiconductor intellectual property (IP) solution, designed for single-chip integration into computer applications. The PCIe2 PHY ssp_x1 includes all the necessary logical, geometric and physical design files to implement complete PCI Express 2.0 physical layer capability for 5Gb/s operation, connecting a host controller or device controller to a PCI Express system.
The PCIe 2.0 PHY supports both the 5 Gbp/s data rate of the PCI Express Gen 2.0 specifications as well as being backwards compatible to the 2.5Gb/s Gen 1.1 specification.

The PCIe 2.0 PHY is fully compliant with all of the required features of the following standards:

- PCI Express Base Specification, Revision 2.0 (including legacy 2.5-Gbps support)
- 5.0 Gbps data rate
- PCI Express Base Specification, Revision 1.1
- 2.5Gbps data rate
- PIPE 3 compliant PCI Express interface

Accessible on SODIMM200 socket:

Clock	PCIE CLK1_P, CLK1_N
Transmit	PCIE TXP, TXN
Receive	PCIE RXP, RXN
Control	PCIE Wake

2.1.13 Adress-Data-Bus realized by the External Interface Module (EIM)

The EIM handles the interface to devices external to the chip, including generation of chip selects, clock and control for external peripherals and memory. It provides asynchronous access to devices with SRAM-like interface and synchronous access to devices with NOR-Flash-like or PSRAM-like interface.

The features of the uSDHC module include the following:

- Up to four chip selects for external devices
- Flexible address decoding. Each chip select memory space determined separately, according to VIA port configuration. Configurable Chip Select 0 base address (by VIA)
- Individual select signal for each one of the memory space defined. Up to 6 memory spaces may be defined and programmed individually.
- 28-bit external address bus, max memory size can be 256MByte (2 Gigabit).
- Selectable Write Protection for each Chip Select
- Support for multiplexed address / data bus operation x16 and x32 port size
- Programmable Data Port Size for each Chip Select (x8, x16 and x32)
- Programmable Wait-State generator for each Chip Select, for write and read accesses separately
- Asynchronous accesses with programmable setup and hold times for control signals
- Support for Asynchronous page mode accesses (x16 and x32 port size)
- Independent synchronous Memory Burst Read Mode support for NOR-Flash and PSRAM memories (x16 and x32 port size)
- Independent synchronous Memory Burst Write Mode support for PSRAM and NORFlash like memories (CellularRAM™ from Micron, Infineon, and Cypress, OneNAND™ and utRAM™ from Samsung, and COSMORAM™ from Toshiba)
- Support of NAND-Flash devices with NOR-Flash like interface - MDOC™ (MSystems), OneNAND™ (Samsung)
- Independent programmable variable/fix Latency support for read and write synchronous (burst) mode
- Support for Big Endian and Little Endian operation modes per access
- ARM AXI slave interface. One ID at a time support.
- External Interrupt support, RDY_INT signal function as external interrupt
- Boot from external device support according to boot signals, using RDY_INT signal
- RDY signal support assertion after reset for MDOC™ (M-Systems) device
- INT signal support assertion after reset for OneNAND™ (Samsung) device

Accessible on SODIMM200 socket:

EIM Control	EIM_RW, EIM_OE, EIM_WAIT, EIM_RD/RW
EIM Address	00-15, 22-25
EIM Address	16-19 (muxed with Bluetooth 3.0+ EDR PCM Audio Signals SAIF)
EIM Address	20-21 (muxed with SPDIF IN and OUT)
EIM Data	00-15
EIM EB	00-03
EIM CS	00-02

2.1.14 24Bit RGB LCD

In the parallel video interfaces (for synchronous access), the data bus has up to 32 bits. Non-trivial mapping of pixels to the bus is restricted to the 24 LSB's. This mapping is fully configurable and very flexible and supports a wide variety of devices from major manufacturers. The interface also supports "generic data". Such data is transferred - byte-by-byte, without modification - between the system memory and the display device (through a serial interface or 8/16-bit parallel interface). Non-conventional pixel formats can be supported by considering them as "generic data".

Features

- Interface clock derived from the IPU internal clock (master mode)
- Interface clock provided by an external source (slave mode)
- up to 24-bit data bus.
- Compatible with MIPI-DPI standard
- Control protocol - follows Sharp HR and generic TFT definitions
- Supports BT.656 (8-bit) and BT.1120 (16-bit) protocols
- Supports HDTV standards SMPTE274 (1080i/p) and SMPTE296 (720p)
- RGB - color depth fully configurable; up to 8 bits/value (color component)
- YUV 4:2:2, 8 bits/value (for TV encoder)
- For synchronous access with one cycle/pixel, this enables, e.g (including 35% blanking intervals)
- 240 Mega-Accesses/Sec if the DI clock is derived from an external to IPU source (like another PLL)
- 266 Mega-Accesses/Sec if the DI clock is derived from the IPU clock (HSP_CLK)
- When off-chip interfaces are involved the rate may be limited by IO capabilities. Screen size: up to 4096 x 2048 pixels, programmable by software.
- Scan Order: progressive or interlaced
- Programmable horizontal and vertical synchronization output signals (for synchronous access)
- Data enabling output signal
- Software contrast control using 8-bit programmable pulse-width modulation (PWM).
  Two dedicated PWM outputs are provided

Accessible on SODIMM200 socket:

Display Data Control:	Data Enable, Clock, HSYNC, VSYNC, \Reset, PWR Enable
Display Backlight Control:	BL_PWM (PWM2), BL Enable,
Display Data	00-17
Display Data	18-23 assembly options: (WLAN MMC1: Data 0-3 + Clock + CMD) muxed with (SPI5: SS 0-2 +MOSI + MISO + SCLK)

2.1.15 Flexible Controller Area Network (FLEXCAN)

The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers is supported. The CAN Protocol Engine (PE) sub-module manages the serial communication on the CAN bus, requesting RAM access for receiving and transmitting message frames, validating received messages and performing error handling. The Controller Host Interface (CHI) sub-module handles Message Buffer selection for reception and transmission, taking care of arbitration and ID matching algorithms. The Bus Interface Unit (BIU) sub-module controls the access to and from the internal interface bus, in order to establish connection to the ARM and to other blocks. Clocks, address and data buses, interrupt outputs and test signals are accessed through the Bus Interface Unit.

The FLEXCAN module includes these distinctive legacy features:

- Version 2.0B
- Standard and Extended data and remote frames
- Zero to eight bytes data length
- Programmable bit rate up to 1 Mb/sec
- Content-related addressing
- Flexible Mailboxes of eight bytes data length. Each Mailbox is configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per Mailbox
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Transmission abort capability
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard or 512 partial (8 bits) IDs, with up to 32 individual masking capability
- 100% backwards compatibility with previous FLEXCAN version
- Unused structures space can be used as general purpose RAM space
- Listen only mode capability, Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts independent of the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power modes, with programmable wake up on bus activity
- Configurable Glitch filter width to filter the noise on CAN bus when waking up
- Remote request frames may be handled automatically or by software.
- Self mechanism for ID filter configuration in Normal Mode
- CAN bit time settings and configuration bits can only be written in Freeze Mode
- Tx mailbox status (Lowest priority buffer or empty buffer)
- SYNC bit status to inform that the module is synchronous with CAN bus
- CRC status for transmitted message
- Selectable priority between Mailboxes and Rx FIFO during matching process

Accessible on SODIMM200 socket:

CAN1	RX, TX	(Attention: TrizepsVII and TrizepsMX28 are not directly compatible! Solution on i-PAN5)
CAN2	RX, TX	(Attention: TrizepsVII and TrizepsMX28 are not directly compatible! Solution on i-PAN5)

2.1.16 Camera (8bit parallel interface) from Image Processing Unit (IPU)

The IPU is planned to be a part of the video and graphics subsystem in an application processor. This is an enhanced version of the IPUv1. The goal of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. The role of these camera ports is to receive input from image sensors (or TV decoders) and to provide support for time-sensitive control signals to the camera. (Non-time-sensitive controls; configuration, reset are performed by the ARM platform through I2C I/F or GPIO signals).

The camera port includes the following features:

- Direct connectivity to most relevant image sensors and to TV decoders.
- 8-bit input data bus with programmable polarity.
- Scan order: progressive or interlaced data (expected only for YUV 4:2:2) is sent directly to system memory, where it can be read back for further processing.
- Frame size: up to 8192 x 4096 pixels
- Average: up to 180M pixels/sec Bayer - 90 M pixels/sec (e.g., 9M pixels @ 15 fps) YUV 4:2:2 - 45 M pixels/sec (e.g., 3 M pixels @ 15 fps) YUV 4:4:4 or RGB - 30 M pixels/sec (e.g., 3M pixels @ 10 fps)
- Peak: up to pixels/sec (to account for up to 35% blanking intervals)
- Synchronization signals are received using either of the following methods: Dedicated control signals -VSYNC, HSYNC - with programmable pulse width & polarity, Controls embedded in the data stream, following loosely the BT.656 protocol, with flexibility in code values and location. The image capture is triggered by the ARM platform or by an external signal (such as a mechanical shutter).
- Frame rate reduction, by the periodic skipping of frames
- The supported reduction ratios are: m:n, where m,n<=5, supported independently for the different destinations - IC, SMFC.
- Window-of-interest selection, Pre-flash - for red-eye reduction and for measurements (such as focus) in lowlight conditions

Accessible on SODIMM200 socket:

Camera Data	0-7 (CIF_DAT12 – CIF_DAT18)
Camera Control	CIF_VSYNC, CIF_HSYNC, CIF_MCLK, CIF_PCLK

2.2 PMIC (Power Managment IC)

The Trizeps-VII module uses a single power supply of +3V3. To generate the different voltages needed for the i.MX6, DDR3, Storage, Ethernet and Audio a highly integrated 14 Channel Configurable Power Management Integrated Circuit is used. The PMPF0100 is the Power Management Integrated Circuit (PMIC) designed primarily for use with Freescale's i.MX6 series of application processors. The core voltage can be adjusted dynamically through a dedicated I2C interface.

Features of the PMPF100:

- Four to six configurable buck regulators for supply to the processor core, memory and other peripherals
- Boost regulator for OTG support
- Six Programmable LDO regulators
- LDO/Switch supply for RTC/SNVS support on i.MX processors
- DDR Memory reference voltage
- Power control logic with processor interface and event detection
- I2C bus for control & register access
- Coin cell charger
- OTP(One time programmable) memory for device configuration
- Programmable start-up sequence and timing
- Battery backed-up memory
- Programmable Standby and Sleep modes

2.2.1 Lesswire WiBear 11n WLAN and Bluetooth

The Trizeps VII can be delivered with a combined wireless-module which offers WLAN and Bluetooth coexistence support. The WiBear11n industrial universal module is designed for both simultaneous and independent operation of the following: 802.11a/b/g/n payload data rates for Wireless Local Area Network (WLAN), Bluetooth 3.0+High Speed (HS) and Bluetooth 2.1+EDR. It provides a complete end-to-end solution for lowpower applications. It includes an integrated MAC/Baseband processor and RF front-end components and can connect to a host processor through SDIO interface. Two UFL-antenna connectors are used to attach external antennas. The UFL-connector in the edge is for BlueTooth and the connector which is placed further in the middle is for WLAN.

Features of the radio module:

- Standards: IEEE 802.11a/b/g/n/e/i/h/d/k/r/w
- WLAN 802.11a/b/g/n station and micro access point operation (up to 8 clients supported)
- 802.11n 1x1 SISO
- 802.11 PHY data rates up to 72 Mbps (20 MHz channel) and up to 150 Mbps (40 MHz channel)
- Hardware 64- and 128-bit encryption AES engine performance
- Embedded security supplicant
- WAPI encryption is supported by hardware
- Background scan mode
- Bluetooth 3.0 + HS (High Speed)
- Bluetooth 2.1 + EDR (backward compatibility)
- Wide temperature operation range -40°C to +85°C
- Compact 14.8mm x 14.8mm footprint, surface mounting
- SDIO high speed interface
- Support for low power modes
- CE/FCC/IC compliant (pending)

Accessible on SODIMM200 socket:

PCM Audio Signals SAIF	(muxed with EIM Address 16-19)
WLAN MMC1	Data 0-3 + Clock + CMD (muxed with SPI5: SS 0-2 +MOSI + MISO + SCLK assembly option with Display Data 18-23)
WLAN_PWDN	

2.3 Interfaces of the i.MX 6 high-speed 60pol. FX11 board to board connector

The Trizeps-VII Module offers the following additional interfaces:

2.3.1 Camera (MIPI fast serial two lane interface) from Image Processing Unit (IPU)

The IPU is planned to be a part of the video and graphics subsystem in an application processor. This is an enhanced version of the IPUv1. The goal of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. The role of these camera ports is to receive input from image sensors (or TV decoders) and to provide support for time-sensitive control signals to the camera. (Non-time-sensitive controls; configuration, reset are performed by the ARM platform through I2C I/F or GPIO signals).

The camera port includes the following features:

- High-speed serial interface - MIPI (Mobile Industry Processor Interface) CSI-2 (Camera Serial Interface) (implemented partly in the IPU and partly in the HSC).
- Up to four data lanes; up to 800 Mbps per lane
- Class 1 compliancy (supporting all primary formats)
- Interleaved color components, up to 16 bits per value (component).
- Average: up to 120M values/sec, 1.44 Gbps Bayer - 120M pixels/sec (e.g., 8M pixels @ 15 fps, 12 bits per value) YUV 4:2:2 - 60M pixels/sec (e.g., 4M pixels @ 15 fps, 12 bits per value) YUV 4:4:4 or RGB - 40M pixels/sec (e.g., 4 pixels @ 10 fps, 12 bits per value) Peak: up to 160 values/sec, 1.92 Gbps (to account for up to 35% blanking intervals)

Accessible on FX11 B2B connector:

Camera clock lane	CSI_CLKN, CLKP
Camera data lanes	CSI_D0N, D0P, D1N, D1P

2.3.2 Low Voltage Differential Signaling Displays

There are 2 LVDS channels (LVDS0 and LVDS1). These outputs are used to communicate RGB data and controls to external LCD displays.

The LVDS ports may be used as follows:

- Single channel output up to 165 Mpixels/sec
- Dual channel output (one input source, two channels outputs for two displays) up to 85 MP/sec (for example, WUXGA at 60 Hz) each.
- Split channel output (one input source, splitted to 2 channels on output)
- Separate 2 channel output (2 input sources from IPU).

Accessible on FX11 B2B connector:

LVDS0 clock lane	LVDS0_CLKN, CLKP
LVDS0 data lanes	LVDS0_TX0N, TX0P, TX1N, TX1P, TX2N, TX2P, TX3N, TX3P
LVDS1 clock lane	LVDS1_CLKN, CLKP
LVDS1 data lanes	LVDS1_TX0N, TX0P, TX1N, TX1P, TX2N, TX2P, TX3N, TX3P

2.3.3 10/100/1000-Mbps Ethernet MAC (ENET)

The core implements a triple speed 10/100/1000 Mbps Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or fullduplex 10/100Mbps Ethernet LANs and full-duplex gigabit Ethernet LANs. The MAC operation is fully programmable and can be used in NIC (Network Interface Card), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819. The core also implements a hardware acceleration block to optimize the performance of network controllers providing IP and TCP, UDP, ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead. The core implements programmable embedded FIFOs that can provide buffering on the receive path for loss-less flow control Advanced power management features are available with magic packet detection and programmable power-down modes. For industrial automation application, the IEEE 1588 standard is becoming the main technology for precise time synchronization on Ethernet networks. This provides accurate clock synchronization for distributed control nodes to overcome one of the drawbacks of Ethernet.
The programmable 10/100/1000 Ethernet MAC with IEEE 1588 integrates a standard IEEE 802.3 Ethernet MAC with a time-stamping module.

Ethernet MAC Features

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking
- Dynamically configurable to support 10/100 Mbps and Gigabit operation
- Supports 10/100 Mbps full duplex and configurable half duplex operation
- Supports gigabit full duplex operation
- Compliant with the AMD magic packet detection with interrupt for node remote power management
- Seamless interface to commercial ethernet PHY device via: a 4-bit Medium Independent Interface (MII) operating at 25 MHz, or a 2-bit Reduced MII (RMII) operating at 50 MHz, or a (double data rate) 4-bit Reduced GMII (RGMII) operating at 125 MHz.
- Simple 64-Bit FIFO interface to user application
- CRC-32 checking at full speed with optional forwarding of the frame check sequence (FCS) field to the client
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis when operating in full duplex mode
- Implements automated pause frame (802.3 x31A) generation and termination providing flow control without user application intervention
- Pause quanta used to form pause frames, dynamically programmable
- Pause frame generation additionally controllable by user application offering flexible traffic flow control
- Optional forwarding of received pause frames to the user application
- Implements standard flow-control mechanism
- In half-duplex mode, provides full collision support, including jamming, backoff, and automatic retransmission
- Support for VLAN-tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)
- Programmable promiscuous mode support to omit MAC destination address checking on receive
- Multicast and unicast address filtering on receive based on 64 entries hash table reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length
- Statistics indicators for frame traffic and errors (alignment, CRC, length) and pause frames providing for IEEE 802.3 basic and mandatory management information database (MIB) package and remote network monitoring (RFC 2819)
- Simple handshake user application FIFO interface with fully programmable depth and threshold levels
- Separate status word available for each received frame on the user interface providing information such as frame length, frame type, VLAN tag, and error information
- Multiple internal loopback options

- MDIO master interface for PHY device configuration and management with two programmable MDIO base addresses
- Supports legacy FEC buffer descriptors

Accessible on FX11 B2B connector:

Transmit path	RGMII_TXC, TD0, TD1, TD2, TD3, TX_CTL
Receive path	RGMII_RXC, RD0, RD1, RD2, RD3, RX_CTL
Serial management signals	MDIO, MDC

2.3.4 Serial Advanced Technology Attachment Controller (SATA)

The chip includes an integrated Serial Advanced Technology Attachment (SATA) controller that is compatible with the Advanced Host Controller Interface (AHCI) specification.The SATA Controller block (SATA) along with integrated physical link hardware (SATA PHY) provide one SATA port for the attachment of external SATA compliant storage devices.

The SATA block supports the following features:

- Compliant with the following specifications:
- Serial ATA 3.0
- AHCI Revision 1.3
- AMBA 2.0 from ARM
- SATA 1.5 Gb/s and SATA 3.0 Gb/s speed.
- eSATA (external analog logic also needs to support eSATA)
- RX data buffer for recovered clock systems
- Data alignment circuitry when RX data buffer is also included
- OOB signaling detection and generation
- 8b/10b encoding/decoding
- Asynchronous signal recovery, including retry polling
- Power management features including automatic partial-to-slumber transition
- BIST loopback modes
- Supports one SATA device(port0)
- Configurable AMBA AHB interface (one master and one slave for each interface)
- Internal DMA engine
- Hardware-assisted Native Command Queuing for up to 32 entries
- Port Multiplier with command-based switching
- Disabling RX and TX Data clocks during power down modes

Accessible on FX11 B2B connector:

SATA data lanes	SATA_RXN, PXP, TXN, TXP

2.3.5 High Definition Multimedia Interface (HDMI)

The High Definition Multimedia Interface (HDMI) is a wired digital interconnect that replaces the analog TV out or VGA out. HDMI is capable of transferring uncompressed video, audio, and data using a single cable. The video pixel rates are typically from 25 MHz up to 297 MHz (4k x 2k and 3D video modes), but HDMI can support higher rates up to 340 MHz. It can support S/PDIF (IEC60958 L-PCM and IEC61937 compressed non-linear PCM: AC-3, MPEG-1/-2 Audio, DTSR, MPEG-2/-4 AAC, ATRAC, WMA, MAT) and Parallel HBR (high bit rate) audio interface, enabling the support of DolbyR True-HD and DTS-HD Master Audio. HDMI has the capability of automatically setting the display format configuration (intelligent link). HDMI include a content protection system called HDCP (High-bandwidth Data Content Protection). The HDMI connections can be used to connect DVD recorders, set-top boxes, and game consoles to flat panel televisions and an AV amplifier that can act as repeater/router. HDMI system architecture consists of sources (transmitter) and sinks (receiver). As shown in the figure below, the HDMI cable and connectors carry four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA Data Display Channel (DDC). The DDC is used for configuration and status exchange between a single source and a single sink. The optional CEC protocol provides high-level control functions between all of the various audiovisual products in a user's environment. Audio, video, and auxiliary data is transmitted across the three TMDS data channels. A TMDS clock running at 1x (24-bit true color mode), 1.25x (30-bit Deep color mode), 1.5x (36-bit deep color mode) or 2x (48-bit Deep-Color mode) the video pixel rate is transmitted on the TMDS clock channel and used by the receiver as a frequency reference for data recovery on the three TMDS data channels. Video data can have a pixel size of 24, 30, 36, or 48 bits. Video at the default 24-bit color depth is carried at a TMDS clock rate equal to the pixel clock rate. Higher color depths are carried using a correspondingly higher TMDS clock rate. Video formats with TMDS rates below 25MHz (such as, 13.5MHz for 480i/NTSC) can be transmitted using a pixel-repetition scheme. The video pixels can be encoded in either RGB, YCBCR 4:4:4, or YCBCR 4:2:2 formats.
HDMI uses a packet structure to transmit audio and auxiliary data across the TMDS channels. To attain the highest reliability required of audio and control data, this data is protected with a BCH error correction code and is encoded using a special error reduction code to produce the transmitted 10-bit word. Basic audio functionality consists of a single IEC 60958 L-PCM audio stream (two audio channels) at sample rates of 32 KHz, 44.1 KHz, or 48 KHz, which can accommodate any normal stereo stream. Optionally, HDMI can carry audio at sample rates up to 192KHz and with three to eight audio channels. HDMI can also carry an IEC 61937 compressed (such as, surround sound) audio stream at bit rates up to 24.576 Mbps. For bit rates above 6.144 Mbps, compressed audio streams conforming to IEC 61937 are carried using HBR Audio Stream Packets. Each packet carries four IEC 60958 frames, which corresponds to (4x2x16 =) 128 contiguous bits of an IEC 61937 stream. The source uses the DDC to read the sink's Enhanced Extended Display Identification Data (E-EDID) to obtain the sink's configuration and/or capabilities. The HDMI TX Controller schedules the three periods: Video Data Period, Data Island period, and Control period. During the Video Data Period, the active pixels of an active video line are transmitted. During the Data Island period, audio and auxiliary data are transmitted using a series of packets. The Control period is used when no video, audio, or auxiliary data needs to be transmitted. A Control Period is required between any two periods that are not Control Periods.

HDMI TX includes the following features:

- Supported video formats:
- All CEA-861-E video formats up to 1080p at 60Hz and 720p/1080i at 120Hz
- Supported colorimetry: 24/30/36/48-bit RGB 4:4:4, 24/30/36/48-bit YCbCr 4:4:4, 16/20/24-bit YCbCr 4:2:2, xvYCC601, xvYCC709
- Integrated color space converter: RGB(4:4:4) to/from YCbCr(4:4:4 or 4:2:2)
- Optional HDMI 1.4a supported video formats: All CEA-861-E video formats up to 1080p at 120Hz, HDMI 1.4a 4K x 2K video formats, HDMI 1.4a 3D video modes with up to 340MHz (TMDS clock)
- Optional HDMI 1.4a supported colorimetry: sYCC601, Adobe RGB, Adobe YCC601
- Optional HDMI 1.4a supported Infoframes: Audio InfoFrame packet extension to support LFE playback level information, AVI infoFrame packet extension to support YCC Quantization range (Limited Range, Full Range), AVI infoFrame packet extension to support Content type (Graphics, Photo, Cinema, Game)
- Supported Audio formats: Up to four I2S interface for eight-channel Linear-PCM audio, S/PDIF interface for linear and non-linear PCM formats: AC-3, MPEG-1/-2 Audio, DTS, MPEG- 2/-4 AAC, ATRAC, WMA, MAT
- Parallel audio interface for High-Bit Rate (HBR) Audio: DolbyR True-HD, DTSR-HD Master Audio, Generic Parallel Audio interface, AHB DMA Audio interface, Up to 192 KHz IEC60958 audio sampling rate
- Pixel clock from 13.5MHz up to 340 MHz

- Option to remove pixel repetition clock (prepclk) from HDMI TX interface for an easy integration with third-party HDMI TX PHYs
- Flexible synchronous enable per clock domain to set functional power down modes
- Register access: AMBA AHB, I2C DDC, EDID block read mode
- Advanced PHY testability
- Integrated CEC hardware engine

Accessible on FX11 B2B connector:

HDMI clock lane	HDMI_CLKN, CLKP
HDMI data lane	HDMI_D0N, D0P, D1N, D1P, D2N, D2P
HDMI control signals	HDMI_HPD, CEC_IN

2.3.6 MIPI Serial Display Interface

The DSI Host Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification, providing an interface between the System and the MIPI D-PHY, allowing the communication with a MIPI DSI compliant Display.

The MIPI DSI Host Controller supports the following features:

- Compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.01.00 - 21 February 2008
- Fully Compliant with MIPI Alliance Standard for Display Pixel Interface (DPI-2),
- Version 2.00 15 September 2005 with Pixel Data bus width up to 24bits
- Compliant with MIPI Alliance Standard for Display Bus Interface (DBI-2) Version 2.00 - 29 November 2005. Supported DBI types are: Type B
- 16bit, 9bit and 8bit Data bus width
- DBI and DPI interface can coexist but only one is operational
- Support all commands defined in MIPI Alliance Specification for Display Command
- Set (DCS), Version 1.02.00 - 23 July 2009
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI
- Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009;
- Supports up to 2 D-PHY Data Lanes:
- Bidirectional Communication and Escape Mode Support through Data Lane 0.
- Programmable display resolutions, from 160x120(QQVGA) to 1024x768(XVGA).
- Multiple Peripheral Support capability, configurable Virtual Channels.
- Video Mode Pixel Formats, 16bpp(5,6,5 RGB), 18 bpp(6,6,6,RGB) packed, 18
- bpp(6,6,6,RGB) loosely, 24 bpp(8,8,8,RGB).
- Supports the transmission of all generic commands;
- ECC and Checksum capabilities;
- End of Transmission Packet (EoTp) support;
- Supports ultra low power mode
- Schemes for fault recovery.

Accessible on FX11 B2B connector:

Display clock lane	DSI_CLKN, CLKP
Display data lanes	DSI_D0N, D0P, D1N, D1P

3.0 Firmware:

The Trizeps-VII is delivered with a bootloader which offers an easy way to install or update an operating system by using the µSD-card or USB-OTG. For more informations refer to the Keith & Koep service website: www.keith-koep.com.

3.1 Bootstrap procedure

After reset the processor starts the code of its internal boot-rom. After detecting a valid bootloader on µSD or eMMC, its loaded into RAM. This bootloader decides if to load and run other images or to enter the bootloader-console. The boot-loader-console communication goes via UART1_RXD (P.33), UART1_TXD (P.35). You can find more information about booting on the services-pages at www.keith-koep.com.

4.0 DC operating conditions

1. Supply voltage +3.3 V

2. Typical operating current @1.1GHz (Quad Core), 1GByte DDR3-1066

Running	tbd.
Idle	tbd.
Suspend	tbd.

Please also refer to „20130526_AN_TrizepsVII_PowerSupply_and_Startup.pdf“. (NDA required!)

5.0 Ordering Information

Articlenumber	Description
37100.IT	i.MX6 Solo, Industrial, 800 MHz, 512 MB DDR3-800 32 Bit, µSD Socket, FX11 B2B
37220.EC	i.MX6 Solo, Ext. Consumer, 1 GHz MHz, 1 GByte DDR3-800 32 Bit, µSD Socket, FX11 B2B, WLAN & BT
37300.IT	i.MX6 DualLite, Industrial, 800 MHz, 512 MB DDR3-800 32 Bit, µSD Socket, FX11 B2B
37500.AT	i.MX6 Dual, Automotive, 800 MHz, 512 MB DDR3-800 32 Bit, µSD Socket, FX11 B2B
37700.AT	i.MX6 Quad, Automotive, 1 GHz, 1 GByte DDR3-1066 64 Bit, µSD Socket, FX11 B2B
37800.AT	i.MX6 Quad, Automotive, 1 GHz, 1 GByte DDR3-1066 64 Bit, µSD Socket, FX11 B2B, WLAN & BT

6.0 Pinout information and description

All of the significant signals are accessible via the 200-pin SODIMM socket like previous Trizeps Modules before. Additional high-speed interfaces are accesible to the new 60pol. FX11 connector. For detailed information about pinmux options and compatibility to previous Trizeps versions, please refer to the actual “sodimm200_standard” excel table in the service area of our website:
http://www.keith-koep.com/service/doku.php/service
We recommend the 200pol. SODIMM connector by Tyco Electronics with the part number 1376408-1 and the 60pol.

Please also refere to „sodimm200_standard_v7.xls“, which lists PinMUX options and reset conditions.

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket) (+3V3 GPIO Voltage)

Pin	Name	Description
1	MIC_OUT	microphone input signal
2	AD3	analog voltage input channel 3
3	MIC_GND	microphone ground
4	AD2	analog voltage input channel 2 (battery monitor)
5	LINEIN_L	Line in left channel
6	AD1	analog voltage input channel 1
7	LINEIN_R	Line in right channel
8	AD0	analog voltage input channel 0
9	AUDIO_AGND	Analog ground audio
10	VDDA_AUDIO	Analog power audio
11	AUDIO_AGND	Analog ground audio
12	VDDA_AUDIO	Analog power audio
13	HEADPHONE_GND	Line out ground output Note: Do not tie this pin to Ground. Voltage level is half of VDDA_AUDIO
14	TSPX	positive X-plate touch screen
15	HEADPHONE_L	Line out left channel
16	TSMX	negative X-plate touch screen
17	HEAPHONE_R	Line out right channel
18	TSPY	positive Y-plate touch screen
19	UART4_RXD	UART4 Receive Data
20	TSMY	negative Y-plate touch screen
21	UART4_TXD	UART4 Transmit Data
22	VDDOTP	PMIC program pin (+8V) (only for internal use!)
23	GPIO_7_7	GPIO Emulation: UART2_DTR
24	\USB_OTG_CHD	USB OTG Charge LED Mounting option. In default not connected
25	UART2_CTS	UART2 Clear To Send
26	$\overline{\text{RESET\_IN}}$	reset input (active low)
27	UART2_RTS	UART2 Ready To Send
28	SPEAKER_R	8R Speaker right channel. Mounting option. In default not connected.
29	GPIO_6_14	GPIO Emulation: UART2_DSR
30	SPEAKER_L	8R Speaker left channel. Mounting option. In default not connected.

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket) (+3V3 GPIO Voltage)

Pin	Name	Description
31	GPIO_6_15	GPIO Emulation: UART2_DCD
32	UART1_CTS	UART1 Clear To Send
33	UART2_RXD (Boot Messages)	UART2 Receive Data
34	UART1_RTS	UART1 Ready To Send
35	UART2_TXD (Boot Messages)	UART2 Transmit Data
36	UART1_RXD	UART1 Receive Data
37	GPIO_1_5	GPIO Emulation: UART2_RI
38	UART1_TXD	UART1 Transmit Data
39	GND	Ground
40	+3V3	Power Supply
41	GND	Ground
42	+3V3	Power Supply
43	IRQ	General purpose I/O, capable of waking the system.
44	LCD_EN/BIAS/DRDY	LCD controller data ready
45	GPIO_2_3	General purpose I/O
46	LCD_DAT7	LCD controller display data
47	SD2_CLK	sd/mmc clock
48	LCD_DAT9	LCD controller display data
49	CSIO_DAT12	camera data 0
50	LCD_DAT11	LCD controller display data
51	SD2_DAT3	sd/mmc data 3
52	LCD_DAT12	LCD controller display data
53	CSIO_DAT13	camera data 1
54	LCD_DAT13	LCD controller display data
55	IRQ_USB_SLAVE_CD	usb-slave cable detect irq.
56	LCD_PCLK	LCD controller display data
57	CSIO_DAT14	camera data 2
58	LCD_DAT3	LCD controller display data
59	SD2_CD	sd/mmc detect irq.
60	LCD_DAT2	LCD controller display data
61	CSIO_DAT15	camera data 3
62	LCD_DAT8	LCD controller display data
63	CSIO_DAT16	camera data 4
64	LCD_DAT15	LCD controller display data
65	CSIO_DAT17	camera data 5
66	LCD_DAT14	LCD controller display data
67	CSIO_DAT18	camera data 6, GPIO
68	LCD_HSYNC	LCD line clock
69	GPIO_6_9	GPIO
70	LCD_DAT1	LCD controller display data

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket) (+3V3 GPIO Voltage)

Pin	Name	Description
71	CSIO_DAT19	camera data 7, GPIO
72	LCD_DAT5	LCD controller display data
73	\DISP_BL_EN	LCD Backlight Enable, GPIO
74	LCD_DAT10	LCD controller display data
75	GPIO_5_28	GPIO
76	LCD_DAT0	LCD controller display data
77	PWM1	LCD Backlight PWM, GPIO
78	LCD_DAT4	LCD controller display data
79	GPIO_2_4	Power-Supply voltage drop detect, GPIO
80	LCD_DAT6	LCD controller display data
81	SD2_DAT1	sd/mmc data 1
82	LCD_VSYNC	LCD controller display data
83	GND	Ground
84	+3V3	Power Supply
85	SD2_DAT2	sd/mmc data 2
86	CSIO_VSYNC/SPI1_SSO	camera vertical sync, serial port frame
87	$\overline{\text{RESET\_OUT}}$	Reset output
88	CSIO_MCLK/SPI1_SCLK	camera master clock, serial port clock
89	EIM_RW	Memory Write Enable
90	CSIO_PCLK/SPI1_MISO	camera pixel clock, serial port receive
91	EIM_OE	camera pixel clock, serial port receive
92	CSIO_HSYNC/SPI1_MOSI	camera horizontal sync, serial port transmit
93	GPIO_5_29	read/write direction control for memory bus
94	I2C1_SCL	I2C1 Clock
95	EIM_WAIT	Ready (VLIO-memory-access)
96	I2C1_SDA	I2C1 Data
97	CAN1_RX	CAN1 receive pin
98	\WLAN_PWDN_3V3	GPIO, WLAN/BT Powerdown
99	CAN1_TX	CAN2 transmit pin
100	LCD_PWR_EN	LCD power enable
101	CAN2_RX	CAN2 receive pin
102	\LCD_RESET	LCD reset
103	CAN2_TX	CAN2 transmit pin
104	GPIO_2_27	GPIO
105	\CS2	static chip select
106	\CS3	static chip select
107	EIM_CS0	static chip select
108	+3V3	Power Supply
109	GND	Ground
110	EIM_DA8	memory address bus
111	EIM_DA0	memory address bus
112	EIM_DA9	memory address bus

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket) (+3V3 GPIO Voltage)

Pin	Name	Description
113	EIM_DA1	memory address bus
114	EIM_DA10	memory address bus
115	EIM_DA2	memory address bus
116	EIM_DA11	memory address bus
117	EIM_DA3	memory address bus
118	EIM_DA12	memory address bus
119	EIM_DA4	memory address bus
120	EIM_DA13	memory address bus
121	EIM_DA5	memory address bus
122	EIM_DA14	memory address bus
123	EIM_DA6	memory address bus
124	EIM_DA15	memory address bus
125	EIM_DA7	memory address bus
126	EIM_EB0	SDRAM DQM for data byte 0
127	USB_OTG_PEN	USB OTG +5V Enable
128	EIM_EB1	SDRAM DQM for data byte 1
129	USB_HOST_PEN	USB Host +5V Enable
130	EIM_EB2	SDRAM DQM for data byte 2
131	USB_HOST_OC	Over current detect for USB-Port 1 (Host)
132	EIM_EB3	SDRAM DQM for data byte 3
133	USB_OTG_OC	Over current detect for USB-Port 2 (OTG)
134	EIM_A25	memory address bus
135	USB_OTG_VBUS_5V	Vbus (+5V) for USB-OTG-Port
136	EIM_A24	memory address bus
137	USB_OTG_ID	USB ID Pin (on USB OTG connectors)
138	EIM_A23	memory address bus
139	USB_OTG_DP	Data line for port 2 (USB-OTG)
140	EIM_A22	memory address bus
141	USB_OTG_DN	Data line for port 2 (USB-OTG)
142	EIM_A21	memory address bus
143	USB_HOST_DP	Data line for port 1 (USB-Host)
144	EIM_A20	memory address bus
145	USB_HOST_DN	Data line for port 1 (USB-Host)
146	EIM_A19/PCM_IN	memory address bus/Bluetooth Audio In
147	GND	Ground
148	+3V3	Power Supply
149	EIM_D16	memory data
150	LCD_DAT16	LCD controller display data
151	EIM_D17	memory data
152	LCD_DAT17	LCD controller display data
153	EIM_D18	memory data
154	PCIE_WAKE	PCI-Express Wake

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket) (+3V3 GPIO Voltage)

Pin	Name	Description
155	EIM_D19	memory data
156	PMIC LDO +1V8	LDO output for low current applications
157	EIM_D20	memory data
158	PCIE_CLK1_N	PCI-Express Clock
159	EIM_D21	memory data
160	PCIE_CLK1_P	PCI-Express Clock
161	EIM_D22	memory data
162	PCIE_TXP	PCI-Express transceiver pin
163	EIM_D23	memory data
164	PCIE_TXN	PCI-Express transceiver pin
165	EIM_D24	memory data
166	PCIE_RXP	PCI-Express receiver pin
167	EIM_D25	memory data
168	PCIE_RXN	PCI-Express receiver pin
169	EIM_D26	memory data
170	LCD_D21/SD1_D0/SPI2_MISO	LCD controller display data, MMC1 Data 0
171	EIM_D27	memory data
172	LCD_D20/SD1_D1/SPI2_SS0	LCD controller display data, MMC1 Data 1
173	EIM_D28	memory data
174	LCD_D19/SD1_D2/SPI2_SS1	LCD controller display data, MMC1 Data 2
175	EIM_D29	memory data
176	LCD_D18/SD1_D3/SPI2_SS2	LCD controller display data, MMC1 Data 3
177	EIM_D30	memory data
178	LCD_D23/SD1_CLK/SPI2_SCLK	LCD controller display data, MMC1 Clock
179	EIM_D31	memory data
180	LCD_D22/SD1_CMD/SPI2_MOSI	LCD controller display data, MMC1 Command
181	GND	Ground
182	+3V3	Power Supply
183	\ENET1_LINK_AKT	Link LED signal
184	PCM_OUT/EIM_A18	memory address bus , Bluetooth Audio Out
185	\ENET1_SPEED	Speed LED signal
186	PCM_CLK/EIM_A17	memory address bus , Bluetooth Audio Clock
187	ENET1_TXN	TP TX Output
188	PCM_SYNC/EIM_A16	memory address bus , Bluetooth Audio Sync
189	ENET1_TXP	TP TX Output
190	SD2_CMD	sd/mmc command
191	ENET1_AGND	Analog Ground
192	SD2_DAT0	sd/mmc data 0
193	ENET1_RXN	TP RX Input
194	I2C2_SDA	I2C2 data
195	ENET1_RXP	TP RX Input
196	I2C2_SCL	I2C2 clock

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket) (+3V3 GPIO Voltage)

Pin	Name	Description
197	GND	Ground
198	+3V3	Power Supply
199	GND	Ground
200	RTC_LICELL (oder +3V3)	Supply for RTC Support

TABLE 2. Pinout information of the FX11 bord to board connector of the Trizeps-VII Module (HIROSE FX11A-60P/6-SV0.5(71))

Pin	Name	Description
1	RGMII_RXC	10 / 100 / 1000 Mbit Ethernet
2	SATA_RXN	SATA Interface
3	RGMII_TD3	10 / 100 / 1000 Mbit Ethernet
4	SATA_RXP	SATA Interface
5	RGMII_RD2	10 / 100 / 1000 Mbit Ethernet
6	SATA_TXN	SATA Interface
7	RGMII_RD1	10 / 100 / 1000 Mbit Ethernet
8	SATA_TXP	SATA Interface
9	RGMII_RD0	10 / 100 / 1000 Mbit Ethernet
10	LVDS1_TX2_P	LVDS1 Display
11	GND	Ground
12	GND	Ground
13	RGMII_TD0	10 / 100 / 1000 Mbit Ethernet
14	LVDS1_TX2_N	LVDS1 Display
15	RGMII_TX_CTL	10 / 100 / 1000 Mbit Ethernet
16	LVDS1_TX3_N	LVDS1 Display
17	RGMII_TXC	10 / 100 / 1000 Mbit Ethernet
18	LVDS1_TX3_P	LVDS1 Display
19	RGMII_RX_CTL	10 / 100 / 1000 Mbit Ethernet
20	LVDS1_CLK_P	LVDS1 Display
21	RGMII_TD2	10 / 100 / 1000 Mbit Ethernet
22	LVDS1_CLK_N	LVDS1 Display
23	RGMII_RD3	10 / 100 / 1000 Mbit Ethernet
24	LVDS1_TX0_P	LVDS1 Display
25	RGMII_TD1	10 / 100 / 1000 Mbit Ethernet
26	LVDS1_TX0_N	LVDS1 Display
27	ENET_MDC_3V3	10 / 100 / 1000 Mbit Ethernet
28	LVDS1_TX1_P	LVDS1 Display
29	ENET_MDIO_3V3	10 / 100 / 1000 Mbit Ethernet
30	LVDS1_TX1_N	LVDS1 Display
31	DSI_D1P / ENET_REF_CLK	MIPI Display Interface or 10 / 100 / 1000 Mbit Ethernet
32	DSI_D1N	MIPI Display Interface
33	GND	Ground

Pin	Name	Description
34	GND	Ground
35	LVDS0_TX1_N	LVDS0 Display
36	DSI_CLK0N	MIPI Display Interface
37	LVDS0_TX1_P	LVDS0 Display
38	DSI_CLK0P	MIPI Display Interface
39	LVDS0_TX0_P	LVDS0 Display
40	HDMI_D1P	HDMI Display Interface
41	LVDS0_TX0_N	LVDS0 Display
42	HDMI_D1N	HDMI Display Interface
43	LVDS0_CLK_N	LVDS0 Display
44	HDMI_D2P	HDMI Display Interface
45	LVDS0_CLK_P	LVDS0 Display
46	HDMI_D2N	HDMI Display Interface
47	LVDS0_TX2_P	LVDS0 Display
48	HDMI_HPD	HDMI Display Interface
49	LVDS0_TX2_N	LVDS0 Display
50	HDMI_CLKN	HDMI Display Interface
51	LVDS0_TX3_P	LVDS0 Display
52	HDMI_CLKP	HDMI Display Interface
53	LVDS0_TX3_N	LVDS0 Display
54	HDMI_CEC_IN	HDMI Display Interface
55	GND	Ground
56	GND	Ground
57	DSI_D0N	MIPI Display Interface
58	HDMI_D0N	HDMI Display Interface
59	DSI_D0P	MIPI Display Interface
60	HDMI_D0P	HDMI Display Interface
61	CSI_D0N	MIPI Camera Interface
62	CSI_CLK0N	MIPI Camera Interface
63	CSI_D0P	MIPI Camera Interface
64	CSI_CLK0P	MIPI Camera Interface
65	CSI_D1P	MIPI Camera Interface
66	CSI_D1N	MIPI Camera Interface

Voltage Levels of board to board connector signals:

2.5V LVDS, SATA, HDMI, RGMII, MIPI DSI, MIPI CSI

3.3V MDIO, MDC, (MIPI DSI, MIPI CSI possible)

TABLE 3. Pinout information of the JTAG connector of the Trizeps-VII Module (JST 08FHJ-SM1-TB, 8-pin contact)

Pin	Name	Description
1	+3V3	Power Supply
2	GND	Ground

Pin	Name	Description
3	TMS	JTAG test mode select
4	$\overline{\text{TRST}}$	JTAG test interface reset
5	TCK	JTAG test clock
6	TDO	JTAG test data output
7	TDI	JTAG test data input
8	$\overline{\text{RESET}}$	Reset input

Appendix

7.0 Dimensions of the Trizeps-VII Module

Figure 3. Dimensions (mm) of the Trizeps-VII Module (top view)

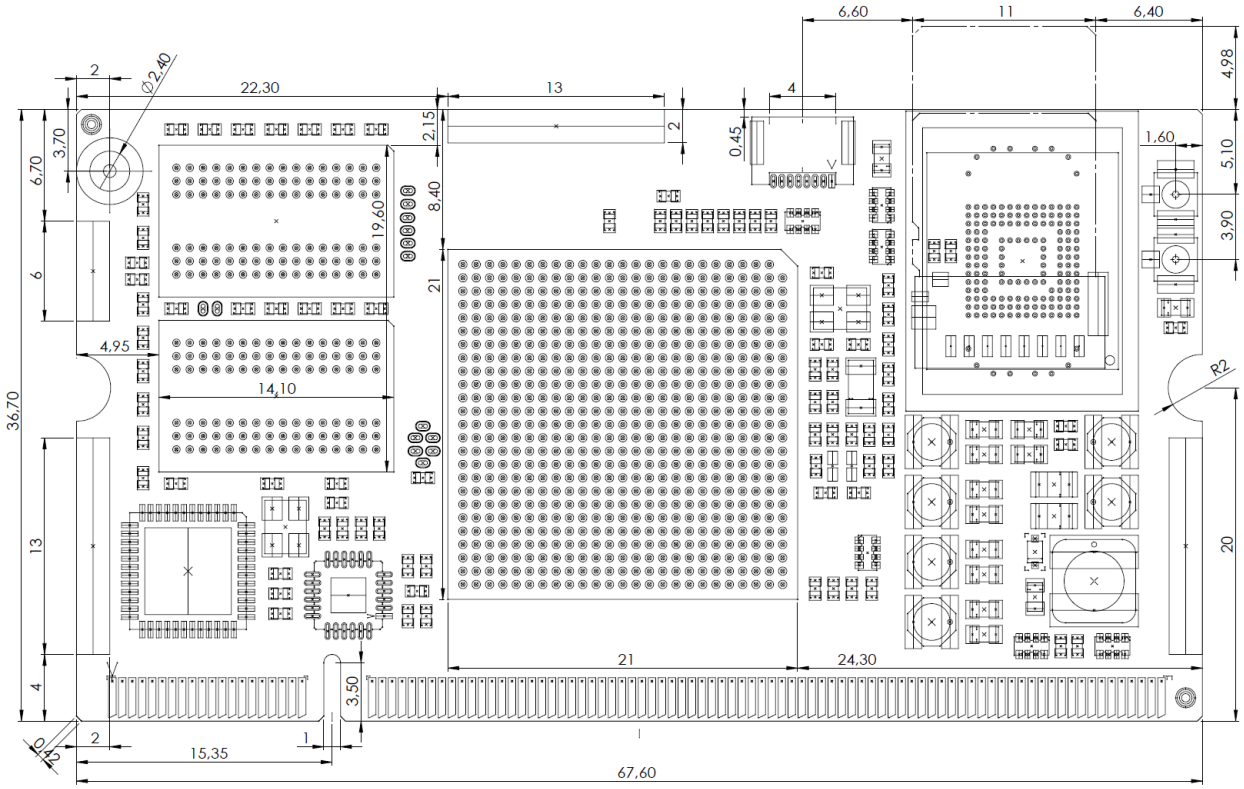


Figure 4. Detail A of Figure 2

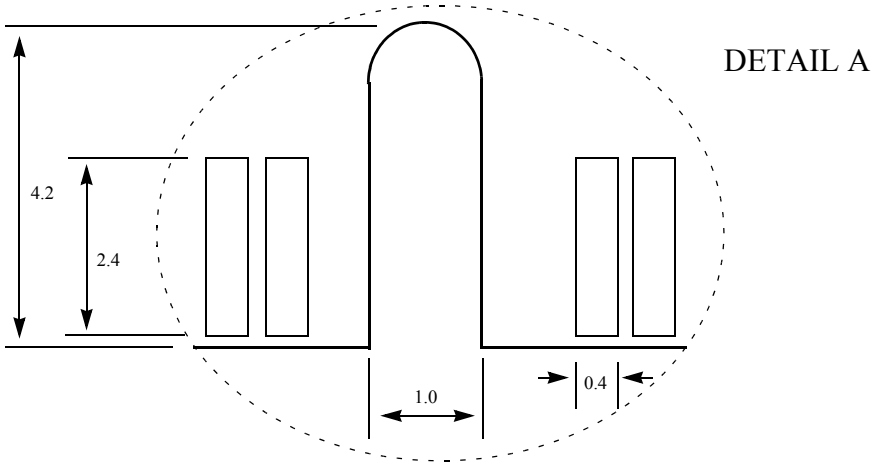
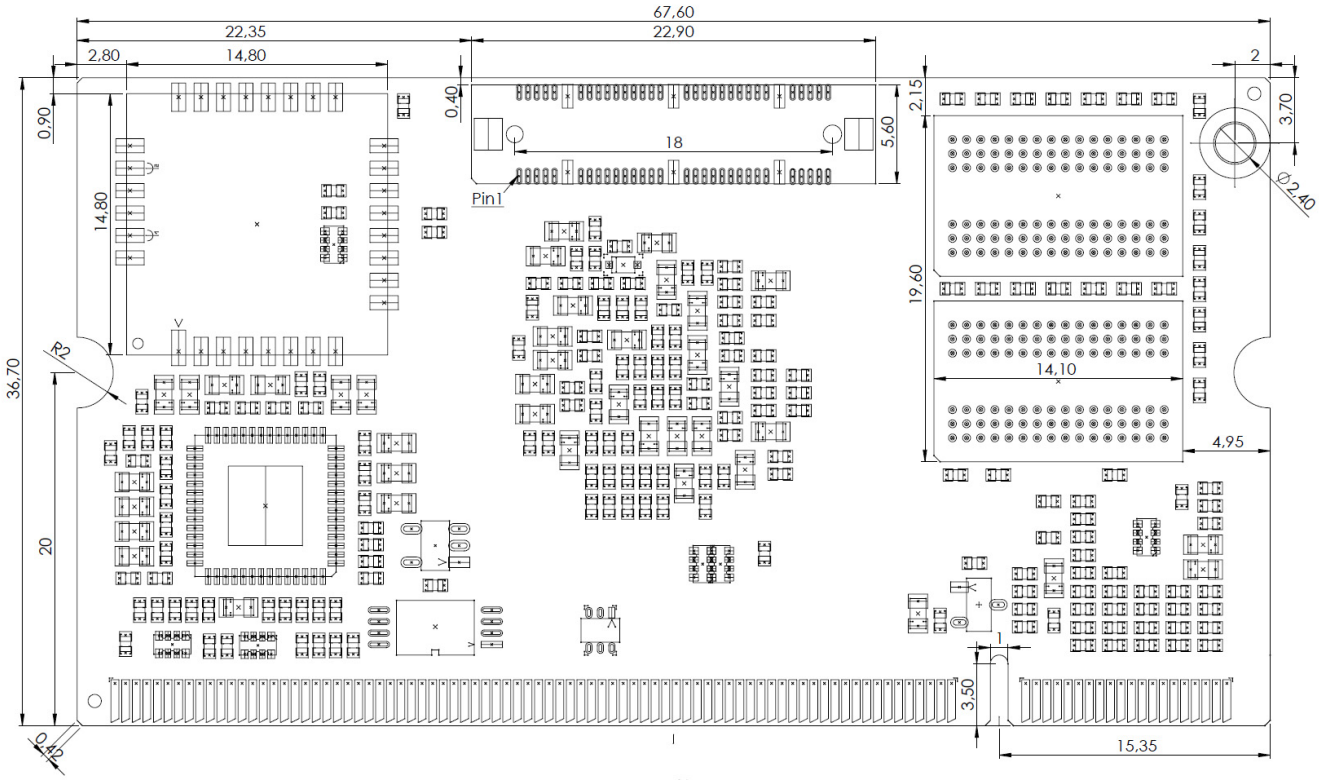


Figure 5. Dimensions of the Trizeps-VII Module (bottom view)



The maximum height is 4.0 mm above the top side and 3.0 mm below the bottom side.

Revision

Board: Trizeps-VII Rev 2

Revision	PCB number	Date	Changes
1.1	TrizepsVIIV1R1L1	05.11.2012	Initial Version
1.2	TrizepsVIIV1R2L1	25.06.2013	Interim Version with corrected B2B-FX11 Pinning
2.0	TrizepsVIIV1R2L1	26.06.2013	Complete Documentation for TrizepsVII_V1R2L1
2.0.1	TrizepsVIIV1R2L1	12.09.2013	Ordering Information modified
2.0.2	TrizepsVIIV1R2L1	09.10.2013	Pin Description in Table 1 rectified
2.0.3	TrizepsVIIV1R2L1	20.11.2013	Ordering Information modified
2.0.4	TrizepsVIIV1R2L1	20.12.2013	Pin Description in Table 2 rectified
2.0.5	TrizepsVIIV1R2L1	16.01.2014	ADC-wiring (Figure 2) added
2.0.6	TrizepsVIIV1R2L1	10.02.2014	Description of UFL-connector position (chapter 2.2.1)
2.0.7	TrizepsVIIV1R2L1	16.05.2014	Pin Name and Description in Table 1 rectified
2.0.8	TrizepsVIIV1R2L1	26.11.2014	Add note for signal HEADPHONE_GND in table 1
2.0.9	TrizepsVIIV1R2L1	23.03.2015	Pin Description in Table 1 rectified