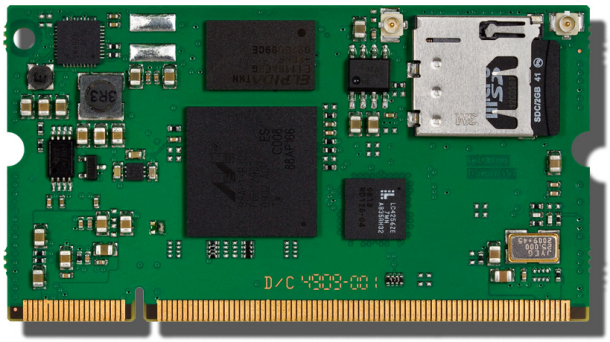
Trizeps-VI Module (V2.0.1)



1.0 Introduction

The Trizeps VI Module is based on the Marvell® Sheeva™ Core CPU 88AP16x ARM® Architecture v.5TE compliant and application code compatible with Intel® SA-1110 and XScale PXA processors which are used on all previous Trizeps-modules. The CPU core is powered by Marvell Sheeva technology scalable beyond 1 GHz that with direct path to commodity DDR2 SDRAM memory for fast user responsiveness and differentiation to bring advanced applications to mainstream devices at low power-consumption. A mutlimedia coprocessor powered by Intel® Wireless MMX™ 2 technology and a graphics engine support HD video and rich GUIs. Some features of the PXA16x: Integrated southbridge support for standard peripherals, NAND, USB2.0 HS OTG w/PHY, SD/SDIO/MMC card, PCIe® (88AP168 only) and a 10/100 Ethernet MAC with PHY on Trizeps VI. The Marvell PXA168 also supports high-resolution displays up to WUXGA and Marvell Qdeo™ Color Intelligent Color Remapping technology. Trizeps VI includes also the Wolfson WM9715L. On a single chip it combines audio codec functions, a touch-screen controller and power management interfaces. The incorporated A/D converter and the touch screen interface provides complete control and read-out of a 4 wire resistive touch screen.

Features of Trizeps VI

Marvell 88AP16x 800/1066MHz	802.11b/g WLAN, Bluetooth
256MB NAND-Flash	WM9715L codec with Audio and Touch
uSD-Card-Socket.	10/100 MBit Ethernet
16 Bit DDR2 (128 MB..256MB)	High-Eff. switching voltage regulator
128/256 Macrocell CPLD	Pin compatible to TRIZEPS III,IV and V

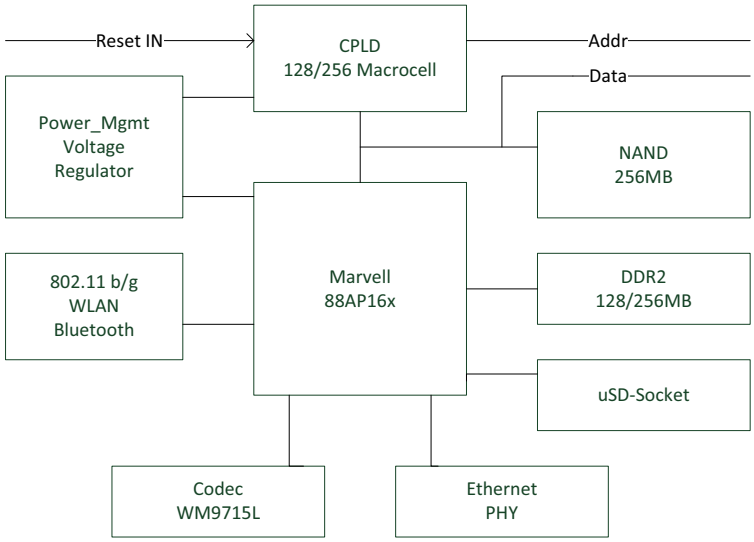
2.0 Functional description of the Trizeps-VI Module

In the following you'll find special information about the Trizeps VI Module. For more information concerning the 88AP16x, WM9715L peripherals please refer to the manufacturers original manuals:

PXA320 http://www.marvell.com
WM9715Lhttp://www.wolfsonmicro.com

For more details about the Trizeps VI, please also see the documentation at http://www.keith-koep.com/service/doku.php/de/service

Figure 1. Trizeps-VI Module



Components of the Trizeps-VI Module:

1. Marvell® 88AP16x (microprocessor)
2. WM9715L (a single chip, stereo audio codec equipped with touch screen and power management interfaces)
3. DDR2 800/1066, 16-Bit wide
4. NAND-Flash @ ND_CS0
5. 10/100MBit Ethernet Phy
6. Switching-mode voltage regulator with I^2C management interface
7. uSD Socket, 2nd SDIO Interface (also wired to SODIMM)
8. 128/256 Macrocell CPLD.
9. 802.11 b/g WLAN, Bluetooth option

2.1 Interfaces of the 88AP16x on SODIMM socket

The Trizeps-VI Module offers the following interfaces:

2.1.1 Universal Asynchronous Receiver / Transmitter (UART) serial ports

The PXA16x processor has 3 UARTs.

The UARTs share the following features:

- Functionally compatible with the 16550
- Ability to add or delete standard asynchronous communications bits (start, stop and parity) in the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator that allows the internal clock to be divided by 1 to (2^{16}-1) to generate an internal 16X clock
- Modem control pins that allow flow control through software

UART1: All of the modem signals are accessible on the SODIMM socket.

UART2: The signals TxD, RxD, CTS and RTS are accessible on the SODIMM sokket.

UART3: The signals RXD and TXD are accessible on the SODIMM socket. This port is routed through the CPLD and shared with the internal Bluetooth-module.

2.1.2 Universal Serial Bus (USB) Host and OTG-Controller

The PXA16x has one dedicated USB Host Port and one USB OTG Port. The OTG-port can function as host or device-port. Both ports support USB2.0 High-Speed.

2.1.3 I²C Bus Interface Unit

The I²C bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the I²C bus. The I²C bus unit allows the PXA16x to serve as a master and slave device that resides on the I²C bus.

The I²C unit enables the PXA16x to communicate with I²C peripherals and microcontrollers for system management functions. The I²C bus requires a minimum amount of hardware to relay status and reliability information concerning the PXA16x subsystem to an external device.

The I²C unit is a peripheral device that resides on the PXA16x internal bus. Data is transmitted to and received from the I²C bus via a buffered interface. Control and status information is relayed through a set of memory-mapped registers. Refer to *The I²C-Bus Specification* for complete details on I²C bus operation.

2.1.4 MultiMediaCard /SD/SDIO-Card Controller

The PXA16x has two SD Host controller, each supporting 2 SD-card sockets.

The MMC/SD/SDIO controller acts as a link between the software that accesses the PXA16x processor and the MMC stack (a set of memory cards) and supports Multimedia Card, Secure Digital, and Secure Digital I/O communications protocols. The SD-Card controller features:

- SD 2.0 specification compliant with two-socket support
- High-speed mode supported with max clock frequeny of 48MHz SD/SDIO and 52MHz for MMC

- Two modes of operation: MMC/SD/SDIO mode and SPI mode. MMC/SD/SDIO mode supports MMC, SD, and SDIO communications protocols. SPI mode supports the SPI communications protocol.
- 1- and 4-bit data transfers are supported for SD and SDIO communications protocols.
- 1-bit/4-bit/8-bit MMC and CE-ATA
- Support for all valid MMC and SD/SDIO protocol data-transfer modes
- Using the MMC communications protocol, multiple MMC cards are supported.
- Using the SD or SDIO communications protocol, one SD or SDIO card per slot is supported.

2.2 Codec (WM9715L)

Trizeps-VI includes the Wolfson WM9715L. It integrates an AC ’97 Rev. 2.2 interface for communication to the processor.

If you need a detailed description please refer to Wolfson datasheet. For interrupt programming of the codec use GP116 (IRQ). GP116 is a general purpose input/output of the PXA16x.

Features of the WM9715L:

- Integrated AC ’97 Rev. 2.2 interface.
- 18-bit stereo audio codec with Variable Rate Audio, input and output gain, digital sound processing, capable of driving headphones, and connecting to microphone and line level inputs.
- 4-wire resistive touch screen interface circuit supporting position, pressure and plate resistance measurements.
- 12-bit successive approximation ADC with internal track-and-hold circuit and analog multiplexer for touch screen readout and monitoring of four external voltage (3.3 V) sources.
- 3.3 V supply voltage and built-in power saving modes for portable and battery-powered applications.

2.3 Memory

The PXA16x has three different memory spaces: DDR2-SDRAM, Static Memory, and Card Memory. Static Memory is accessed through the on-board CPLD, which decodes the multiplexed address/data-bus of the PXA16x to form the address-pins and 3 chip-selects.

2.4 WLAN & Bluetooth

The Trizeps VI can be delivered with a combined wireless-module which offers 802.11 b/g WLAN and Bluetooth v2.0 + EDR with coexistence support. Two UFL-antenna connectors are used to attach external antennas.

2.5 Ethernet PHY

The Trizeps VI module contains a high performance ethernet-PHY with flexible power management architecture to optimize system power consumption. It features

HP Auto-MDIX, which eliminates the need for special crossover cables. The MAC address is stored in the first page of the NAND-flash (TIM-header).

2.6 Voltage converter

The Trizeps-VI module uses a single power supply of +3V3. To generate the different voltages needed for the PXA16x a highly integrated power supply system with a high efficiency switch-mode voltage converter is used. The core voltage can be adjusted dynamically through a dedicated I^2C interface. There is an option to configure the Trizeps VI to run from a single LiPo-cell or +5V input. Contact Keith & Koep for more information.

2.7 Reset generator

Resetting the board is possible by using the $\overline{\text{RESET\_IN}}$ input or by using the JTAG Reset Input.

2.8 JTAG / Debug Port

The JTAG / Debug port consists of several shift registers, with the destination controlled by the TMS pin and data I/O with TDI / TDO. Two JTAG-ports are available on the Trizeps VI: One for the the PXA16x-processor and one for the CPLD.

The JTAG / Debug port provides two different functionalities:

- Programming Flash memory by pushing data through the shift registers
- Hardware-testing using boundary scan interface according to IEEE 1149.1

3.0 Firmware:

The Trizeps-VI is delivered with a bootloader which offers an easy way to install or update an operating system by using the serial interface, SD-card or USB. For more informations refer to the Keith & Koep service website: www.keith-koep.com.

3.1 Bootstrap procedure

After reset the processor starts the code of its internal boot-rom. After detecting a valid bootloader on NAND-flash, its loaded into RAM. This bootloader decides if to load and run other images or to enter the bootloader-console. The bootloader-console communication goes via UART1_RXD (P.33), UART1_TXD (P.35). You can find more information about booting on the services-pages at www.keith-koep.com.

4.0 DC operating conditions

1. Supply voltage 3.3 V
2. Typical operating current @1066MHz, 128MB DDR2-SDRAM
   Running tbd.
   Idle tbd.
   Suspend tbd.

5.0 Ordering Information

Product description (standard)	Ordering number
1. Trizeps VI/C1100/R128/N512/ETH/CODW/RoHS	36025
2. Trizeps VI/C1100/R256/N512/ETH/CODW/RoHS	36045
3. Trizeps VI/C1100/R128/N512/ETH/WB/CODW/RoHS	36065
4. Trizeps VI/C1100/R256/N512/ETH/WB/CODW/RoHS	36085
5. Trizeps VI/C800/R128/N512/ETH/CODW/RoHS	36125
6. Trizeps VI/C800/R256/N512/ETH/CODW/RoHS	36145
7. Trizeps VI/C800/R128/N512/ETH/WB/CODW/RoHS	36165
8. Trizpes VI/C800/R256/N512/ETH/WB/CODW/RoHS	36185

Explanation:

Trizeps VI/CPU MHz/SDRAM MB/Flashtype MB/Ethernet//WLAN BlueTooth/ Codec/RoHS

Example Position 4: 1100 MHz, 256 MB DDR RAM, 512 MB NAND Flash, Ethernet, WLAN + Bluetooth, Wolfson Codec, RoHS

6.0 Pinout information and description

All of the significant signals are accessible via the 200-pin SODIMM socket.

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket)

Pin	Name	Description
1	MIC_OUT	microphone input signal (WM9715L)
2	AD3	analog voltage input (WM9715L)[a]
3	MIC_GND	microphone ground switch input (WM9715L)
4	AD2	analog voltage input (WM9715L)[a]
5	LINEIN_L	Line in left channel (WM9715L)
6	AD1	analog voltage input (WM9715L)[a]
7	LINEIN_R	Line in right channel (WM9715L)
8	AD0	analog voltage input (WM9715L)[a]
9	VSSA_AUDIO	Analog ground audio (WM9715L)
10	VDDA_AUDIO	Analog power audio (WM9715L)
11	VSSA_AUDIO	Analog ground audio (WM9715L)
12	VDDA_AUDIO	Analog power audio (WM9715L)
13	HEADPHONE_GND	Line out ground output (WM9715L) Note: Do not tie this pin to Ground. Voltage level is half of VDDA_AUDIO
14	TSPX	positive X-plate touch screen (WM9715L)[b]
15	HEADPHONE_L	Line out left channel (WM9715L)
16	TSMX	negative X-plate touch screen (WM9715L)[c]
17	HEAPHONE_R	Line out right channel (WM9715L)
18	TSPY	positive Y-plate touch screen (WM9715L)[d]
19	UART3_RXD	serial port three receive pin (CPLD)
20	TSMY	negative Y-plate touch screen (WM9715L)[e]
21	UART3_TXD	serial port three transmit pin (CPLD)
22	VDD_FAULT	not connected
23	UART1_DTR	Full Function UART DTR (PXA16x, GP112)
24	BATT_FAULT	Main battery is low or removed (PMIC)
25	UART1_CTS	Full Function UART Clear To Send (PXA16x,GP110)
26	$\overline{\text{RESET\_IN}}$	reset input
27	UART1_RTS	Full Function UART Ready To Send (PXA16x,GP109)
28	USBOTG-	Mounting option. In default not connected.
29	UART1_DSR	Full Function UART Data Set Ready (PXA16x, GP104)
30	USBOTG+	Mounting option. In default not connected.
31	UART1_DCD	Full Function UART DCD (PXA16x, GP105)

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket)

Pin	Name	Description
32	UART2_CTS	UART2 Clear To Send (PXA16x, GP123), shared with JTAG_TDI
33	UART1_RXD	Full Function UART Receive Data (PXA16x, GP107)
34	UART2_RTS	UART2 Ready To Send (PXA16x, GP124), shared with JTAG_TMS.
35	UART1_TXD	Full Function UART Transmit Data (PXA16x, GP108)
36	UART2_RXD	UART2 Receive Data (PXA16x,GP36), shared with JTAG_TCK
37	UART1_RI	Full Function UART Ring Indicator (PXA16x, GP111)
38	UART2_TXD	UART2 Transmit Data (PXA16x, GP126), shared with JTAG_TDO
39	GND	Ground
40	+3V3	Power Supply
41	GND	Ground
42	+3V3	Power Supply
43	IRQ	General purpose I/O (PXA16x,GP51)
44	L_DENA_BIAS	LCD controller display data (PXA16x,GP59)
45	PRDY	General purpose I/O (PXA16x,GP113) (CF IRQ)
46	LDD07	LCD controller display data (PXA16x,GP67)
47	MMC_CLK	General purpose I/O (PXA16x,GP29)
48	LDD09	LCD controller display data (PXA16x,GP69)
49	IPOD_DAT0	General purpose I/O (PXA16x,GP45)
50	LDD11	LCD controller display data (PXA16x,GP71)
51	MMC_DAT3	General purpose I/O (PXA16x,GP122)
52	LDD12	LCD controller display data (PXA16x,GP72)
53	IPOD_DAT1	General purpose I/O (PXA16x,GP44)
54	LDD13	LCD controller display data (PXA16x,GP73)
55	GP47	General purpose I/O (PXA16x,GP47)
56	L_PCLK	LCD pixel clock (PXA16x,GP58)
57	IPOD_DAT2	General purpose I/O (PXA16x,GP42)
58	LDD03	LCD controller display data (PXA16x,GP63)
59	MMC_DET (act.Hi)	General purpose I/O (PXA16x,GP53)
60	LDD02	LCD controller display data (PXA16x,GP62)
61	IPOD_DAT3	General purpose I/O (PXA16x,GP41)
62	LDD08	LCD controller display data (PXA16x,GP68)
63	IPOD_DAT4	General purpose I/O (PXA16x,GP40)
64	LDD15	LCD controller display data (PXA16x,GP75)
65	IPOD_DAT5	General purpose I/O (PXA16x,GP39)
66	LDD14	LCD controller display data (PXA16x,GP74)
67	IPOD_DAT6	General purpose I/O (PXA16x,GP38)

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket)

Pin	Name	Description
68	L_LCLK	LCD line clock (PXA16x,GP57)
69	GPIO	General purpose I/O (CPLD)
70	LDD01	LCD controller display data (PXA16x,GP61)
71	IPOD_DAT7	General purpose I/O (PXA16x,GP37)
72	LDD05	LCD controller display data (PXA16x,GP65)
73	GP49	General purpose I/O (PXA16x,GP49)
74	LDD10	LCD controller display data (PXA16x,GP70)
75	GP50	General purpose I/O (PXA16x,GP50)
76	LDD00	LCD controller display data (PXA16x,GP60)
77	$\overline{\text{PCD}}$ PCMCIA Card Detect	General purpose I/O (PXA16x,GP43)
78	LDD04	LCD controller display data (PXA16x,GP64)
79	GPIO52_POWERFAIL	General purpose I/O (PXA16x,GP52)
80	LDD06	LCD controller display data (PXA16x,GP66)
81	MMC_DAT1	General purpose I/O (PXA16x,GP120)
82	L_FCLK	LCD frame clock (PXA16x,GP56)
83	GND	Ground
84	+3V3	Power Supply
85	MMC_DAT2	General purpose I/O (PXA16x,GP121)
86	IPOD_VSYNC	(PXA16x,GP46)
87	$\overline{\text{RESET\_OUT}}$	Reset output
88	IPOD_MCLK	(PXA16x,GP54)
89	$\overline{\text{WE}}$	Memory Write Enable (PXA16x)
90	IPOD_PCLK	(PXA16x,GP55)
91	$\overline{\text{OE}}$	Memory Output Enable (PXA16x)
92	IPOD_HSYNC	(PXA16x,GP48)
93	CPLD_RDWR	General purpose I/O (CPLD)
94	$\overline{\text{PCE1}}$	PCMCIA card enable (low-byte) (PXA16x,GP19)
95	SMC_RDY	General purpose I/O (PXA16x)
96	$\overline{\text{PCE2}}$	PCMCIA card enable (high-byte) (PXA16x,GP20)
97	$\overline{\text{POE}}$	PCMCIA output enable (OE, CPLD)
98	$\overline{\text{PREG}}$	PCMCIA register select (PXA16x,GP30)
99	$\overline{\text{PWE}}$	PCMCIA write enable, (WE, CPLD)
100	PSKTSEL	PCMCIA socket select (CPLD)
101	$\overline{\text{PIOW}}$	PCMCIA I/O write (CPLD)
102	$\overline{\text{PWAIT}}$	PCMCIA wait (PXA16x,GP34)
103	$\overline{\text{PIOR}}$	PCMCIA I/O read (CPLD)
104	$\overline{\text{PIOIS16}}$	I/O select 16 (PXA16x,GP31)
105	$\overline{\text{CS1}}$	static chip select (CPLD)
106	$\overline{\text{CS4}}$	static chip select (CPLD)

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket)

Pin	Name	Description
107	$\overline{CS3}$	static chip select (CPLD)
108	+3V3	Power Supply
109	GND	Ground
110	A08	memory address bus (CPLD)
111	A00	memory address bus (CPLD)
112	A09	memory address bus (CPLD)
113	A01	memory address bus (CPLD)
114	A10	memory address bus (CPLD)
115	A02	memory address bus (CPLD)
116	A11	memory address bus (CPLD)
117	A03	memory address bus (CPLD)
118	A12	memory address bus (CPLD)
119	A04	memory address bus (CPLD)
120	A13	memory address bus (CPLD)
121	A05	memory address bus (CPLD)
122	A14	memory address bus (CPLD)
123	A06	memory address bus (CPLD)
124	A15	memory address bus (CPLD)
125	A07	memory address bus (CPLD)
126	SMC_BE1	Byte Enable for data byte 0 (PXA16x)
127	USBHPEN2 (NC)	Not Connected. Use USBHPEN1.
128	SMC_BE2	Byte Enable for data byte 1 (PXA16x)
129	USBHPEN1	Turn on/off the gang power for all host ports
130	n.c.	not connected
131	USBHPWR1	Over current condition indicator for gang powered host port 1
132	n.c.	not connected
133	USBHPWR2	Over current condition indicator for gang powered host port 2
134	A25	memory address bus (CPLD)
135	OTG_VBUS	Vbus input sampled during HNP/SRP operations by the OTG port
136	A24	memory address bus (CPLD)
137	OTG_ID	Connected to the ID pin of the Mini-AB connector for OTG applications
138	A23	memory address bus (CPLD)
139	USBH2_P	Data line for USB-port 2
140	A22	memory address bus (CPLD)
141	USBH2_N	Data line for USB-port 2
142	A21	memory address bus (CPLD)

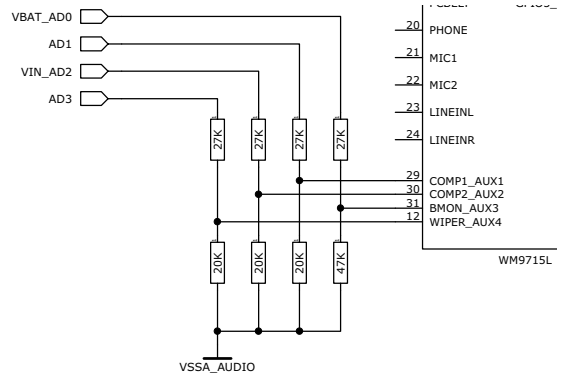
TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket)

Pin	Name	Description
143	USBH1_P	Data line for USB-port 1
144	A20	memory address bus (CPLD)
145	USBH1_N	Data line for USB-port 1
146	A19	memory address bus (CPLD)
147	GND	Ground
148	+3V3	Power Supply
149	D00	memory data (PXA16x)
150	LDD16	General purpose (PXA16x,GP76)
151	D01	memory data (PXA16x)
152	LDD17	General purpose (PXA16x,GP77)
153	D02	memory data (PXA16x)
154	ONE_WIRE	General purpose (PXA17x,GP84)
155	D03	memory data (PXA16x)
156	LD0	1,8V..3,3V LDO voltage-regulator output.
157	D04	memory data (PXA16x)
158	PCIE_CLK	PCI-Express (PXA168 only)
159	D05	memory data (PXA16x)
160	PCIE_CLK_N	PCI-Express (PXA168 only)
161	D06	memory data (PXA16x)
162	PCIE_TX	PCI-Express (PXA168 only)
163	D07	memory data (PXA16x)
164	PCIE_TX_N	PCI-Express (PXA168 only)
165	D08	memory data (PXA16x), opt. used for int. WLAN-chip
166	PCIE_RX	PCI-Express (PXA168 only)
167	D09	memory data (PXA16x), opt. used for int. WLAN-chip
168	PCIE_RX_N	PCI-Express (PXA168 only)
169	D10	memory data (PXA16x), opt. used for int. WLAN-chip
170	LDD21	General Purpose (PXA16x,GP81), MMC4_DAT0 (int. uSD-slot)
171	D11	memory data (PXA16x), opt. used for int. WLAN-chip
172	LDD20	General Purpose (PXA16x,GP80), MMC4_DAT1(int. uSD-slot)
173	D12	memory data (PXA16x), opt. used for int. WLAN-chip
174	LDD19	General Purpose (PXA16x,GP79),MMC4_DAT2(int. uSD-slot)
175	D13	memory data (PXA16x), opt. used for int. WLAN-chip
176	LDD18	General Purpose (PXA16x,GP78),MMC4_DAT3(int. uSD-slot)
177	D14	memory data (PXA16x), opt. used for int. WLAN-chip

TABLE 1. Pinout information of the connector J2 of the Trizeps-VI Module (200-pin SODIMM-socket)

Pin	Name	Description
178	LDD23	General Purpose (PXA16x,GP83),MMC4_CLK(int. uSD-slot)
179	D15	memory data (PXA16x),opt. used for int. WLAN-chip
180	LDD22	General Purpose (PXA16x,GP82), MMC4_CMD(int. uSD-slot)
181	GND	Ground
182	+3V3	Power Supply
183	$\overline{\text{ETH\_LINK\_AKT}}$	Link LED signal (Ethernet-PHY)
184	A18	memory address bus (CPLD)
185	$\overline{\text{ETH\_SPEED100}}$	Speed LED signal (Ethernet-PHY)
186	A17	memory adress bus (CPLD)
187	ETH_TX0-	TP TX Output (Ethernet-PHY)
188	A16	memory adress bus (CPLD)
189	ETH_TX0+	TP TX Output (Ethernet-PHY)
190	MMC_CMD	MultiMedia Card Command (PXA16x, GP28)
191	ETH_AGND	Analog Ground (Ethernet-PHY)
192	MMC_DAT0	MultiMedia Card Data (PXA16x, GP119)
193	ETH_RXI-	TP RX Input (Ethernet-PHY)
194	I2C_DATA	I^2C data (PXA16x, GP102)
195	ETH_RXI+	TP RX Input (Ethernet-PHY)
196	I2C_CLK	I^2C data (PXA16x, GP106)
197	GND	Ground
198	+3V3	Power Supply
199	GND	Ground
200	VCC_BAT	Power Supply VBAT (+3.3V)

a.



b. a 10nF decoupling capacitor against VSSA_AUDIO can be optionally placed

c. a 10nF decoupling capacitor against VSSA_AUDIO can be optionally placed

d. a 10nF decoupling capacitor against VSSA_AUDIO can be optionally placed

e. a 10nF decoupling capacitor against VSSA_AUDIO can be optionally placed

We recommend the 200-pin SODIMM connector by Tyco Electronics with the part number 1376408-1

TABLE 2. Pinout information of the connector J4 of the Trizeps-VI Module (JST 08FHJ-SM1-TB, 8-pin contact)

Pin	Name	Description
1	+3V3	Power Supply
2	GND	Ground
3	TMS	JTAG test mode select (PXA16x)
4	$\overline{\text{TRST}}$	JTAG test interface reset (PXA16x)
5	TCK	JTAG test clock (PXA16x)
6	TDO	JTAG test data output (PXA16x)
7	TDI	JTAG test data input (PXA16x)
8	$\overline{\text{RESET}}$	Reset input (PXA16x)

TABLE 3. Pinout information of the connector J1 of the Trizeps-VI Module (JST 08FHJ-SM1-TB, 8-pin contact)

Pin	Name	Description
1	+1V8	Power Supply
2	GND	Ground
3	TMS	JTAG test mode select (CPLD)
4	n.c.	not connected
5	TCK	JTAG test clock (CPLD)
6	TDO	JTAG test data output (CPLD)
7	TDI	JTAG test data input (CPLD)
8	n.c.	not connected

Appendix

7.0 Dimensions of the Trizeps-VI Module

Figure 2. Dimensions of the Trizeps-VI Module (top view)

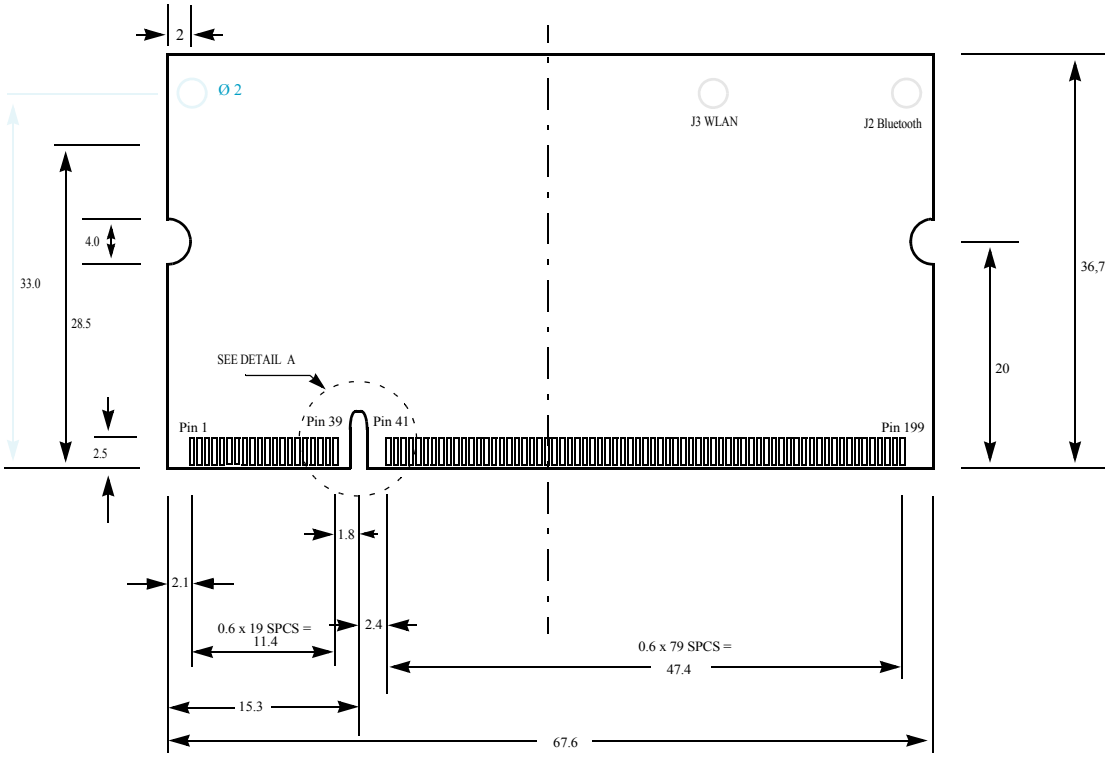


Figure 3. Detail A of Figure 3

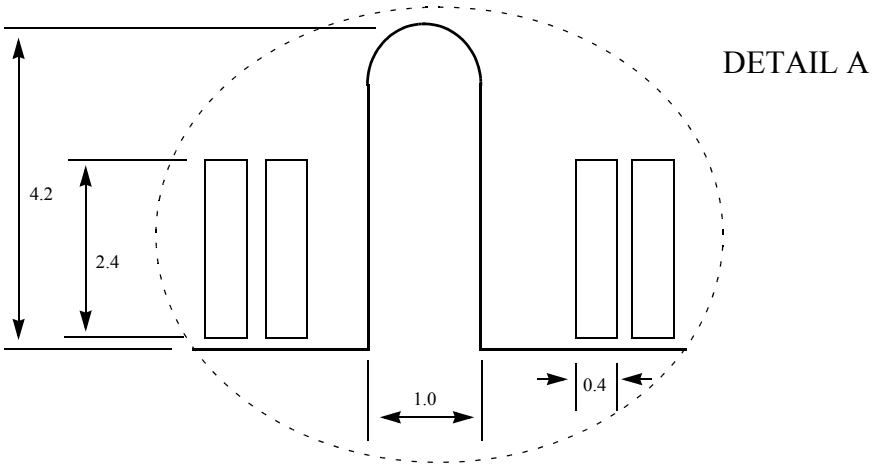
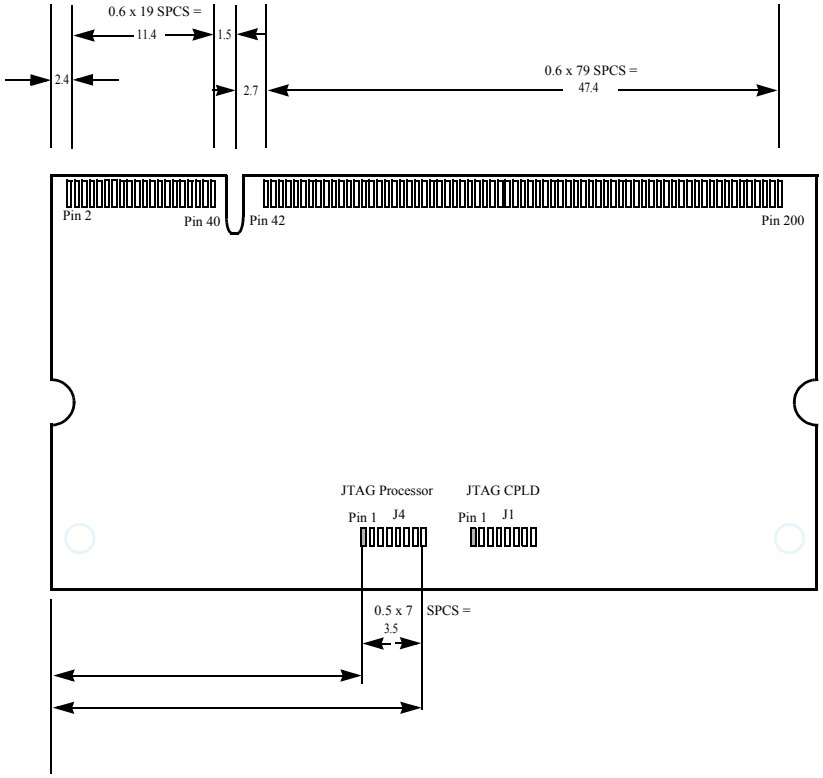


Figure 4. Dimensions of the Trizeps-VI Module (bottom view)



The Maximum height is 4.0 mm above the top side and 2.0 mm below the bottom side.

Revision

Board: Trizeps-VI

Revision	PCB number	Date	Changes
1.0		27.05.2010	Initial Version
2.0		14.02.2013	Codec Change: UCB1400 --> WM9715L
2.0.1		26.11.2014	Add note for signal HEADPHONE_GND in table 1