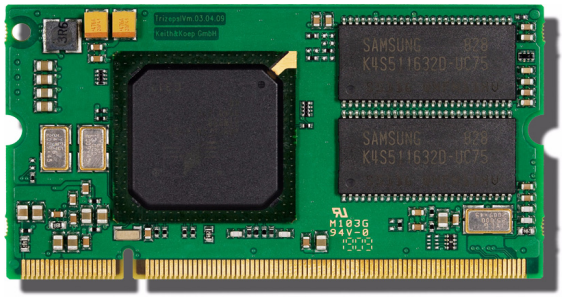
Trizeps-IV-M Module (V1.2.1)



1.0 Introduction

The Trizeps-IV-M Module is based on the Marvell® XScale™ Core CPU PXA270-M (312, 416, 520 + 624 MHz) ARM® Architecture v.5TE compliant and application code compatible with Intel® SA-1110 and PXA255 processor which are used on the Trizeps-I, Trizeps II and Trizeps III Modules. The CPU is based on Intel® Superpipelined RISC technology for high core speeds at low power (860K Dhrystone 2.1 per second @ 520 MHz). It is the first Intel® Personal Internet Client Architecture (PCA) processor to include Intel® Wireless MMX® technology, enabling high performance, low-power multimedia acceleration with a general-purpose instruction set. Intel® Quick Capture technology provides one of the industry´s most flexible and powerful camera interfaces for capturing digital images and video. While performance is key, power consumption is also a critical component. The new capabilities of Wireless Intel SpeedStep® technology provide a quantum leap forward in low-power operation.
Some features of the PXA270-M: Integrated memory and PCMCIA/CompactFlash Controller with 100MHz Memory Bus. System Control Module includes general-purpose interruptible I/O ports, real-time clock, watchdog and interval timers, power management controller, interrupt and reset controller, LCD controller and two on-chip oscillators. Trizeps-IV-M includes also the Wolfson WM9715L , on a single chip it combines audio codec functions, a touch-screen controller and power management interfaces. The incorporated A/D converter and the touch screen interface provides complete control and read-out of a 4 wire resistive touch screen. The onboard 10/100MBit Ethernet Interface offers best of class integration and optimal performance together with the XScale embedded processors.

Features of Trizeps-IV-M

Marvell XScale PXA270-M	
32 Bit Numonyx Strata (P33) Flash 32..64MB	Wolfson WM9715L codec with Audio and Touch
	32 Bit 10/100 MBit Ethernet Controller
32 Bit LP SDRAM (64..128 MB)	High-Eff. switching core-voltage regulator supporting SpeedStep® Features
Reset Generator	Pin compatible to Trizeps III, Trizeps IV

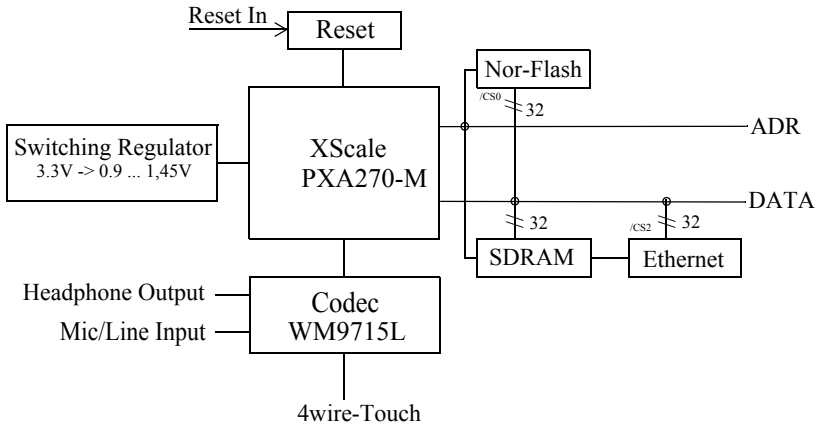
2.0 Functional description of the Trizeps-IV-M Module

In the following you'll find special information about the Trizeps-IV-M Module. For more information concerning the PXA270-M, WM9715L, DM9000 peripherals please refer to the manufacturers original manuals:

PXA270-M
WM9715L
DM9000 http://davicom.co.tw

Components of the Trizeps-IV-M Module

Figure 1. Trizeps-IV-M Module



Components of the Trizeps-IV-M Module:

1. Marvell® XScale PXA270-M (microprocessor)
2. WM9715L (a single chip, stereo audio codec equipped with touch screen and battery monitoring), IRQ GP01
3. SDRAM 32-Bit wide @ bank 0
4. Flash: Numonyx Strata® Flash (P33) 32-Bit wide @ nCS0
5. DM9000 10/100 MBit Ethernet Controller and onboard EEPROM for mac-adr IRQ GP101
6. ISL6271CR switch-mode core voltage regulator with I^2C management interface
7. Reset generator

2.1 Interfaces of the XScale PXA270-M on SODIMM socket

The Trizeps-IV-M Module offers the following interfaces:

2.1.1 Universal Asynchronous Receiver / Transmitter (UART) serial ports

The XScale PXA270-M processor has 3 UARTs: Full Function UART (FFUART), Bluetooth UART (BTUART), and Standard UART (STUART).

The UARTs share the following features:

- Functionally compatible with the 16550
- Ability to add or delete standard asynchronous communications bits (start, stop and parity) in the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator that allows the internal clock to be divided by 1 to (2^{16}-1) to generate an internal 16X clock
- Modem control pins that allow flow control through software

Full Function UART: All of the modem signals are accessible on the SODIMM socket.

Bluetooth UART: The signals TxD, RxD, CTS and RTS are accessible on the SODIMM socket.

Standard UART: The signals IRRxD and IRTxD are accessible on the SODIMM socket. This serial port can work as Fast Infrared Communications Port (FICP). It operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. The FICP is based on the 4-Mbps IrDA standard and uses four-position pulse modulation (4PPM) and a specialized serial packet protocol developed for IrDA transmission. To support the standard, the FICP has:

- A bit Encoder / Decoder
- A serial-to-parallel data engine
- A transmit FIFO 128 entries deep and 8 bits wide
- A receive FIFO 128 entries deep and 11 bits wide

The FICP shares GPIO pins for transmit and receive data with the Standard UART. Only one of the ports can be used at a time.

2.1.2 Universal Serial Bus (USB) Device Controller (UDC)

The UDC supports 16 endpoints and can operate half-duplex at a rate of 12Mbps (as a slave only, not as a host or hub controller). The UDC supports four device configurations. Configurations 1, 2 and 3 each supports two interfaces. This allows the host to accomodate dynamic changes in the physical bus topology. A configuration is a specific combination of USB resources available on the device. An interface is a related set of endpoints that present a device feature or function to the host.

2.1.3 Universal Serial Bus (USB) Host Controller

The PXA270-M has one dedicated USB Host Port and another Port which can be driven as Host or as a combined OTG Port, which supports the dynamic role change between Upstream/Downstream Ports (Host/Function). These ports can be driven with speedgrades FS and LS.

Note: Only 2xUSB-Host or 1xUSB-Host and 1xUSB-Device is supported. WinCE-Software automatically disables USB-Host-Port 2, when an USB-Device-Cable is plugged. Use a hub on USB-Host-Port 1, if additional USB-Host ports are needed.

2.1.4 I²C Bus Interface Unit

The I²C bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the I²C bus. The I²C bus unit allows the PXA270-M to serve as a master and slave device that resides on the I²C bus.

The I²C unit enables the PXA270-M to communicate with I²C peripherals and microcontrollers for system management functions. The I²C bus requires a minimum amount of hardware to relay status and reliability information concerning the PXA270-M subsystem to an external device.

The I²C unit is a peripheral device that resides on the PXA270-M internal bus. Data is transmitted to and received from the I²C bus via a buffered interface. Control and status information is relayed through a set of memory-mapped registers. Refer to *The I²C-Bus Specification* for complete details on I²C bus operation.

2.1.5 MultiMediaCard / SDCard Controller

The MMC/SD/SDIO controller acts as a link between the software that accesses the PXA270-M processor and the MMC stack (a set of memory cards) and supports Multimedia Card, Secure Digital, and Secure Digital I/O communications protocols. The MMC controller supports the MMC system, a low-cost data storage and communications system. The MMC controller in the PXA270-M processor is based on the standards outlined in the *MultiMediaCard System Specification Version 3.2*. The SD controller supports one SD or SDIO card based on the standards outlined in the *SD Memory Card Specification Version 1.01* and *SDIO Card Specification Version 1.0 (Draft 4)*.The MMC controller features:

- Data-transfer rates up to 19.5 Mbps for MMC, 1-bit SD/SDIO, and SPI mode data transfers
- Data-transfer rates up to 78 Mbps for 4-bit SD/SDIO data transfers
- Two modes of operation: MMC/SD/SDIO mode and SPI mode. MMC/SD/SDIO mode supports MMC, SD, and SDIO communications protocols. SPI mode supports the SPI communications protocol.
- 1- and 4-bit data transfers are supported for SD and SDIO communications protocols.
- Support for all valid MMC and SD/SDIO protocol data-transfer modes
- Using the MMC communications protocol, multiple MMC cards are supported.
- Using the SD or SDIO communications protocol, one SD or SDIO card is supported.

2.2 Codec (WM9715L)

Trizeps-IV-M includes the Wolfson WM9715L. It integrates an AC ’97 Rev. 2.2 interface for communication to Marvell® XScale processor.

If you need a detailed description please refer to Wolfson data sheet. For interrupt programming of the codec use GP02 (IRQ). GP02 is a general purpose input/output of the PXA270-M.

Features of the WM9715L:

- Integrated AC ’97 Rev. 2.2 interface.
- 18-bit stereo audio codec with Variable Rate Audio, input and output gain, digital sound processing, capable of driving headphones, and connecting to microphone and line level inputs.
- 4-wire resistive touchpanel interface circuit supporting position, pressure and plate resistance measurements.

- 12-bit successive approximation ADC with internal track-and-hold circuit and analog multiplexer for touch screen readout and monitoring of four external voltage (3.3 V) sources.
-
- 3.3 V supply voltage and two comparator inputs for battery monitoring.

2.3 Memory

The XScale PXA270-M has three different memory spaces: SDRAM, Static Memory, and Card Memory.

2.3.1 SDRAM interface

The PXA270-M supports the SDRAM interface, which supports four 16- and 32-bit-wide SDRAM partitions. Each partition is allocated 64 or 256 MBytes of the internal memory map, but the actual size of each partition depends on the SDRAM configuration.

The Trizeps-IV-M uses the first ($\overline{SDCS}$[0]) of the four partition selects and 32 data-lines. Usually the memory size of SDRAM is 64 MByte, configuration with 128 MByte is also possible.

2.3.2 Static Memory interface / Variable Latency I/O interface

The static memory and variable latency I/O interface has six chip selects ($\overline{CS}$[5:0]) and 26 bits of byte address (A[25:0]) for access up to 64 MBytes of memory in each of six banks. Each chip select is individually programmed for selecting one of the supported static memory types:

- Non-burst ROM or Flash memory is supported on $\overline{CS}$[5:0]
- Burst ROM or Flash (with non-burst writes) is supported on $\overline{CS}$[5:0]
- Burst and non-burst SRAM is supported on $\overline{CS}$[5:0]
- Variable Latency I/O is supported on $\overline{CS}$[5:0]
- Synchronous static memory is supported on $\overline{CS}$[3:0]

The Trizeps-IV-M NOR Flash memory is selected by the first ($\overline{CS}$[0]) of the six chip selects and uses 32 data-lines. Usually the size of Flash memory is 32 MByte, configuration with 64,128 MByte is also possible. Using sizes larger than 64 MByte disables the use of CS[1], where the DiskOnChip Option may be mounted.

2.4 16-Bit PC Card / Compact Flash Interface

The PXA270-M card interface is based on *The PC Card Standard - Volume 2 - Electrical Specification, Release 2.1,* and *CF+ and CompactFlash Specification Revision 1.4.* The 16-bit PC Card / Compact Flash interface provides control signals to support any combination of 16-bit PC Card / Compact Flash for two card sockets, using address line (A[25:0]) and data lines (D[15:0]).

The PXA270-M 16-bit PC Card / Compact Flash Controller provides the following signals:

- $\overline{PREG}$ is muxed with A[26] and selects register space (I/O or attribute) versus memory space
- $\overline{POE}$ and $\overline{PWE}$ allow memory and attributes reads and writes
- $\overline{PIOR}$, $\overline{PIOW}$ and $\overline{PIOIS16}$ control I/O reads and writes

- $\overline{\text{PWAIT}}$ allows extended access times
- $\overline{\text{PCE2}}$ and $\overline{\text{PCE1}}$ are byte select high and low for a 16-bit data bus
- PSKTSEL selects between two card sockets

Keith&Koep uses a small external logic to switch the power to the cardinterface and drive external buffers, which are needed to build a hotplug save system. There is also a buffer to read status signals like the BVDDx and VSx signals. Using the reference schematics, you can be sure to be compatible with Keith&Koep's bootloader and OS adaptions.

2.5 Ethernet Controller (nCS2, GPIO101, 32Bit VLIO)

The Trizeps-IV-M module contains a high performance ethernet controller from Davicom. The MAC address is stored into an on board EEPROM. The chip select is given by nCS2 and the interrupt is made by GPIO101. The WAKEUP pin of the DM9000 is routed to GPIO97. All 32 datalines are connected to use the available bandwith.

2.6 Voltage converter (ISL6271CR)

The Trizeps-IV-M Module uses a single power supply of +3V3. To generate the different voltages needed for the PXA270-M a highly integrated power supply system with a high efficiency switch-mode voltage converter is used. The core voltage can be adjusted dynamically through a dedicated I^2C interface.

2.7 Reset generator

Resetting the board is possible by using the $\overline{\text{RESET\_IN}}$ input or by using the JTAG Reset Input.

2.8 JTAG / Debug Port

The JTAG / Debug port consists of several shift registers, with the destination controlled by the TMS pin and data I/O with TDI / TDO. The JTAG / Debug port provides two different functionalities:

- Programming Flash memory by pushing data through the shift registers
- Hardware-testing using boundary scan interface according to IEEE 1149.1

3.0 Firmware:

The Trizeps-IV-M firmware package includes:

1. PBL (Primary Bootstrap Loader)
2. BOOTP/ TFTP Bootstrap Loader (Keith&Koep). It offers the following features:
   1. BOOTP/TFTP download with Ethernet support
   2. Special download with simple serial protocol
   3. Flash support
   4. On board selftest
   5. SD/MMC Support (including FAT)

3.1 Bootstrap procedure

After reset the processor starts the PBL (Primary Boot Loader). The PBL sets up the memory system and the MMU and decides to enter the Boot Loader or a customer program. The communication goes via FF_RXD (P.33), FF_TXD (P.35). You can find more information about booting using the document „bootloader2.pdf“.

4.0 DC operating conditions

1. Supply voltage 3.3 V
2. Typical operating current @520MHz, with ethernet-controller + DoC

Running	405 mA
Idle	210 mA
Deep Idle	135 mA
Suspend	51.5 mA

3. Typical operating current @312MHz, with ethernet-controller + DoC

Running	285 mA
Idle	190 mA
Suspend	51.5 mA

4. Typical operating current @520MHz, without ethernet-controller

Running	345 mA
Idle	157 mA
Suspend	2 mA

5. Typical operating current @312MHz, without ethernet-controller

Running	210 mA
Idle	127 mA
Suspend	2 mA

4.1 Operating temperature:

standard: 0° ... +70°C
industrial available: -20°...+85°C (Ethernet not included)

4.2 Storage temperature

-40...+125°C

4.3 Humidity

<= 95% (non-condensing) for operating and storage

5.0 Ordering Information

	Product description (standard)	Ordering number
1.	Trizeps IV-M/C312/R64/P33.32/N0/ETH/CODW/RoHS	34413
2.	Trizeps IV-M/C520/R64/P33.32/N0/ETH/CODW/RoHS	34383
3.	Trizeps IV-M/C520/R128/P64.32/N0/ETH/CODW/RoHS	34363

Explanation:
Trizeps IV-M/Cpu MHz/SDRAM MB/Flash type and MB/DiskOnChip type and MB (N0 = not populated)/Ethernet/Codec/RoHS

Example Position 1: 312MHz, 64MB SDRAM, P33 Flash 32MB, DiskOnChip G4 type not populated, Ethernet, Wolfson Codec, ROHS

6.0 Pinout information and description

All of the significant signals are accessible via the 200-pin SODIMM socket.

TABLE 1. Pinout information of the connector J2 of the Trizeps-IV-M Module (200-pin SODIMM-socket)

Pin	Name	Description
1	MIC_OUT	microphone input signal (WM9715L)
2	AD3	analog voltage input (WM9715L)[a]
3	MIC_GND	microphone ground switch input (WM9715L)
4	VIN_AD2	analog voltage input (WM9715L)[a]
5	LINEIN_L	Line in left channel (WM9715L)
6	AD1	analog voltage input (WM9715L)[a]
7	LINEIN_R	Line in right channel (WM9715L
8	VBAT_AD0 opt. AC97_RESET	analog voltage input (WM9715L)[a]
9	VSSA_AUDIO	Analog ground audio (WM9715L)
10	VDDA_AUDIO	Analog power audio (WM9715L)
11	VSSA_AUDIO	Analog ground audio (WM9715L)
12	VDDA_AUDIO	Analog power audio (WM9715L)
13	HEADPHONE_GND	Line out ground output (WM9715L) Note: Do not tie this pin to Ground. Voltage level is half of VDDA_AUDIO
14	TSPX opt. AC97_SYNC	positive X-plate touch screen (WM9715L)[b] opt. direct AC97_SYNC fr. PXA270M
15	HEADPHONE_L	Line out left channel (WM9715L)
16	TSMX opt. AC97_DATAIN	negative X-plate touch screen (WM9715L)[c] opt. direct AC97_DATAIN fr. PXA270M
17	HEAPHONE_R	Line out right channel (WM9715L)
18	TSPY opt. AC97_DATAOUT	positive Y-plate touch screen (WM9715L)[d] opt. direct AC97_DATAOUT fr. PXA270M
19	RXD_2	serial port two receive pin (IrDA) (PXA270-M, GP46)
20	TSMY opt. BITCLK	negative Y-plate touch screen (WM9715L)[e] opt. direct BITCLK fr. PXA270M
21	TXD_2	serial port two transmit pin (IrDA) (PXA270-M,GP47)
22	VDD_FAULT	Main power source goes out of regulation (PXA270-M)
23	FF_DTR	Full Function UART DTR (PXA270-M, GP82)
24	BATT_FAULT	Main battery is low or removed (PXA270-M)
25	FF_CTS	Full Function UART Clear To Send (PXA270,GP09)
26	$\overline{\text{RESET\_IN}}$	reset input
27	FF_RTS	Full Function UART Ready To Send (PXA270-M,GP83)
28	TUDC-	USB Fn bidirectional (UDC) (PXA270-M, USBC_N)

TABLE 1. Pinout information of the connector J2 of the Trizeps-IV-M Module (200-pin SODIMM-socket)

Pin	Name	Description
29	FF_DSR	Full Function UART Data Set Ready (PXA270-M)
30	TUDC+	USB Fn bidirectional (UDC) (PXA270-M, USBC_P)
31	FF_DCD	Full Function UART DCD (PXA270-M, GP10)
32	BT_CTS	BlueTooth UART Clear To Send (PXA270-M, GP44)
33	FF_RXD	Full Function UART Receive Data (PXA270-M, GP96)
34	BT_RTS	BlueTooth UART Ready To Send (PXA270, GP45)
35	FF_TXD	Full Function UART Transmit Data (PXA270, GP16)
36	BT_RXD	BlueTooth UART Receive Data (PXA270,GP42)
37	FF_RI	Full Function UART Ring Indicator (PXA270, GP38)
38	BT_TXD	BlueTooth UART Transmit Data (PXA270, GP43)
39	GND	Ground
40	+3V3	Power Supply
41	GND	Ground
42	+3V3	Power Supply
43	GPIO00_IRQ_PIC	General purpose I/O (PXA270,GP00)
44	L_BIAS	LCD controller display data (PXA270,GP77)
45	GPIO01_PRDY	General purpose I/O (PXA270,GP13) (CF IRQ)
46	LDD07	LCD controller display data (PXA270,GP65)
47	MMC_CLK	General purpose I/O (PXA270,GP32)
48	LDD09	LCD controller display data (PXA270,GP67)
49	CIF_DD0	General purpose I/O (PXA270,GP27)
50	LDD11	LCD controller display data (PXA270,GP69)
51	MMC_DAT3	General purpose I/O (PXA270,GP111)
52	LDD12	LCD controller display data (PXA270,GP70)
53	CIF_DD1	General purpose I/O (PXA270,GP114)
54	LDD13	LCD controller display data (PXA270,GP71)
55	GPIO105_IRQUSB_SL	General purpose I/O (PXA270,GP105)
56	L_PCLK	LCD pixel clock (PXA270,GP76)
57	CIF_DD2	General purpose I/O (PXA270,GP116)
58	LDD03	LCD controller display data (PXA270,GP61)
59	MMC_DET (act.Hi)	General purpose I/O (PXA270,GP12)
60	LDD02	LCD controller display data (PXA270,GP60)
61	CIF_DD3	General purpose I/O (PXA270,GP103)
62	LDD08	LCD controller display data (PXA270,GP66)
63	CIF_DD4	General purpose I/O (PXA270,GP90)
64	LDD15	LCD controller display data (PXA270,GP73)
65	CIF_DD5/UCLK	General purpose I/O (PXA270,GP91)
66	LDD14	LCD controller display data (PXA270,GP72)

TABLE 1. Pinout information of the connector J2 of the Trizeps-IV-M Module (200-pin SODIMM-socket)

Pin	Name	Description
67	CIF_DD6/PWM1	General purpose I/O (PXA270,GP17)
68	L_LCLK	LCD line clock (PXA270,GP75)
69	GPIO85/$\overline{\text{IRQ\_HIL}}$	General purpose I/O (PXA270,GP85)
70	LDD01	LCD controller display data (PXA270,GP59)
71	CIF_DD7 TTLIO_IRQ	General purpose I/O (PXA270,GP108)
72	LDD05	LCD controller display data (PXA270,GP63)
73	CIF_DD8	General purpose I/O (PXA270,GP107)
74	LDD10	LCD controller display data (PXA270,GP68)
75	CIF_DD9	General purpose I/O (PXA270,GP106)
76	LDD00	LCD controller display data (PXA270,GP58)
77	$\overline{\text{PCD}}$ PCMCIA Card Detect	General purpose I/O (PXA270,GP11)
78	LDD04	LCD controller display data (PXA270,GP62)
79	GPIO81_POWERFAIL	General purpose I/O (PXA270,GP81)
80	LDD06	LCD controller display data (PXA270,GP64)
81	MMCDAT1	General purpose I/O (PXA270,GP109)
82	L_FCLK	LCD frame clock (PXA270,GP74)
83	GND	Ground
84	+3V3	Power Supply
85	MMCDAT2	General purpose I/O (PXA270,GP110)
86	CIF_FV	(PXA270,GP24)
87	$\overline{\text{RESET\_OUT}}$	Reset output (PXA270)
88	CIF_MCLK	(PXA270,GP23)
89	$\overline{\text{WE}}$	Memory Write Enable (PXA270)
90	CIF_PCLK	(PXA270,GP26)
91	$\overline{\text{OE}}$	Memory Output Enable (PXA270)
92	CIF_LV	(PXA270,GP25)
93	RD/$\overline{\text{WR}}$	read/write direction control for memory bus (PXA270)
94	$\overline{\text{PCE1}}$	PCMCIA card enable (low-byte) (PXA270,GP102)
95	GPIO18/$\overline{\text{RDY}}$	General purpose I/O (PXA270)
96	$\overline{\text{PCE2}}$	PCMCIA card enable (high-byte) (PXA270,GP54)
97	$\overline{\text{POE}}$	PCMCIA output enable (PXA270,GP48)
98	$\overline{\text{PREG}}$	PCMCIA register select (PXA270,GP55)
99	$\overline{\text{PWE}}$	PCMCIA write enable, $\overline{\text{WE}}$ VLIO (PXA270,GP49)
100	PSKTSEL	PCMCIA socket select (PXA270,GP104)
101	$\overline{\text{PIOW}}$	PCMCIA I/O write (PXA270,GP51)
102	$\overline{\text{PWAIT}}$	PCMCIA wait (PXA270,GP56)
103	$\overline{\text{PIOR}}$	PCMCIA I/O read (PXA270,GP50)
104	$\overline{\text{PIOIS16}}$	I/O select 16 (PXA270,GP57)

TABLE 1. Pinout information of the connector J2 of the Trizeps-IV-M Module (200-pin SODIMM-socket)

Pin	Name	Description
105	$\overline{CS1}$	static chip select (PXA270,GP15)
106	$\overline{CS4}$	static chip select (PXA270,GP80)
107	$\overline{CS3}$	static chip select (PXA270,GP79)
108	+3V3	Power Supply
109	GND	Ground
110	A08	memory address bus (PXA270)
111	A00	memory address bus (PXA270)
112	A09	memory address bus (PXA270)
113	A01	memory address bus (PXA270)
114	A10	memory address bus (PXA270)
115	A02	memory address bus (PXA270)
116	A11	memory address bus (PXA270)
117	A03	memory address bus (PXA270)
118	A12	memory address bus (PXA270)
119	A04	memory address bus (PXA270)
120	A13	memory address bus (PXA270)
121	A05	memory address bus (PXA270)
122	A14	memory address bus (PXA270)
123	A06	memory address bus (PXA270)
124	A15	memory address bus (PXA270)
125	A07	memory address bus (PXA270)
126	DQM0	SDRAM DQM for data byte 0 (PXA270)
127	USBHPEN2 (NC)	Not Connected. Use USBHPEN1.
128	DQM1	SDRAM DQM for data byte 1 (PXA270)
129	USBHPEN1	Turn on/off the gang power for all host ports
130	DQM2	SDRAM DQM for data byte 2 (PXA270)
131	USBHPWR1	Over current condition indicator for gang powered host ports
132	DQM3	SDRAM DQM for data byte 3 (PXA270)
133	USBHPWR2 (NC)	Vbus pulsing control
134	A25	memory address bus (PXA270)
135	OTG_VBUS	Vbus input sampled during HNP/SRP operations by the OTG port
136	A24	memory address bus (PXA270)
137	OTG_ID	Connected to the ID pin of the Mini-AB connector for OTG applications
138	A23	memory address bus (PXA270)
139	USBH_P2	Data line for port 2
140	A22	memory address bus (PXA270)

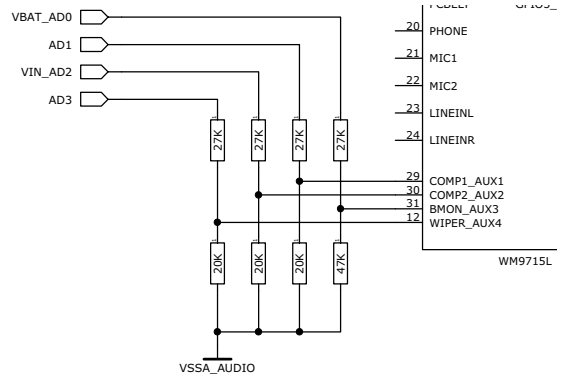
TABLE 1. Pinout information of the connector J2 of the Trizeps-IV-M Module (200-pin SODIMM-socket)

Pin	Name	Description
141	USBH_N2	Data line for port 2
142	A21	memory address bus (PXA270)
143	USBH_P1	Data line for port 1
144	A20	memory address bus (PXA270)
145	USBH_N1	Data line for port 1
146	A19	memory address bus (PXA270)
147	GND	Ground
148	+3V3	Power Supply
149	D00	memory data (PXA270)
150	D16 opt: LDD16	memory data (PXA270)
151	D01	memory data (PXA270)
152	D17 opt: LDD17	memory data (PXA270)
153	D02	memory data (PXA270)
154	D18	memory data (PXA270)
155	D03	memory data (PXA270)
156	D19	memory data (PXA270)
157	D04	memory data (PXA270)
158	D20 opt: LCS	memory data (PXA270)
159	D05	memory data (PXA270)
160	D21 opt: LVSYNC	memory data (PXA270)
161	D06	memory data (PXA270)
162	D22 opt:UIO	memory data (PXA270)
163	D07	memory data (PXA270)
164	D23 opt:UEN	memory data (PXA270)
165	D08	memory data (PXA270)
166	D24 opt: UDET	memory data (PXA270)
167	D09	memory data (PXA270)
168	D25	memory data (PXA270)
169	D10	memory data (PXA270)
170	D26	memory data (PXA270)
171	D11	memory data (PXA270)
172	D27	memory data (PXA270)
173	D12	memory data (PXA270)
174	D28	memory data (PXA270)
175	D13	memory data (PXA270)
176	D29	memory data (PXA270)
177	D14	memory data (PXA270)
178	D30	memory data (PXA270)

TABLE 1. Pinout information of the connector J2 of the Trizeps-IV-M Module (200-pin SODIMM-socket)

Pin	Name	Description
179	D15	memory data (PXA270)
180	D31	memory data (PXA270)
181	GND	Ground
182	+3V3	Power Supply
183	$\overline{\text{ETH\_LINK\_AKT}}$	Link LED signal (DM 9000)
184	A18	memory address bus (PXA270)
185	$\overline{\text{ETH\_SPEED100}}$	Speed LED signal (DM 9000)
186	A17	memory adress bus (PXA270)
187	ETH_TX0-	TP TX Output (DM 9000)
188	A16	memory adress bus (PXA270)
189	ETH_TX0+	TP TX Output (DM 9000)
190	MMC_CMD	MultiMedia Card Command (PXA270)
191	ETH_AGND	Analog Ground (DM 9000)
192	MMC_DAT	MultiMedia Card Data (PXA270)
193	ETH_RXI-	TP RX Input (DM 9000)
194	I2C_DATA	I^2C data (PXA270, GP118)
195	ETH_RXI+	TP RX Input (DM 9000)
196	I2C_CLK	I^2C data (PXA270, GP117)
197	GND	Ground
198	+3V3	Power Supply
199	GND	Ground
200	VCC_BAT	Power Supply VBAT PXA270 (+3.3V)

a.



b. a 10nF decoupling capacitor against VSSA_AUDIO can be optionally placed

c. a 10nF decoupling capacitor against VSSA_AUDIO can be optionally placed

d. a 10nF decoupling capacitor against VSSA_AUDIO can be optionally placed

e. a 10nF decoupling capacitor against VSSA_AUDIO can be optionally placed

We recommended the 200-pin SODIMM connector by Tyco Electronics with the part number 1376408-1

TABLE 2. Pinout information of the connector J4 of the Trizeps-IV Module (JST 08FHJ-SM1-TB, 8-pin contact)

Pin	Name	Description
1	+3V3	Power Supply
2	GND	Ground
3	TMS	JTAG test mode select (PXA255)
4	$\overline{\text{TRST}}$	JTAG test interface reset (PXA255)
5	TCK	JTAG test clock (PXA255)
6	TDO	JTAG test data output (PXA255)
7	TDI	JTAG test data input (PXA255)
8	$\overline{\text{RESET}}$	Reset input (PXA255)

7.0 Dimensions of the Trizeps-IV-M Module

Figure 2. Dimensions of the Trizeps-IV-M Module (top view)

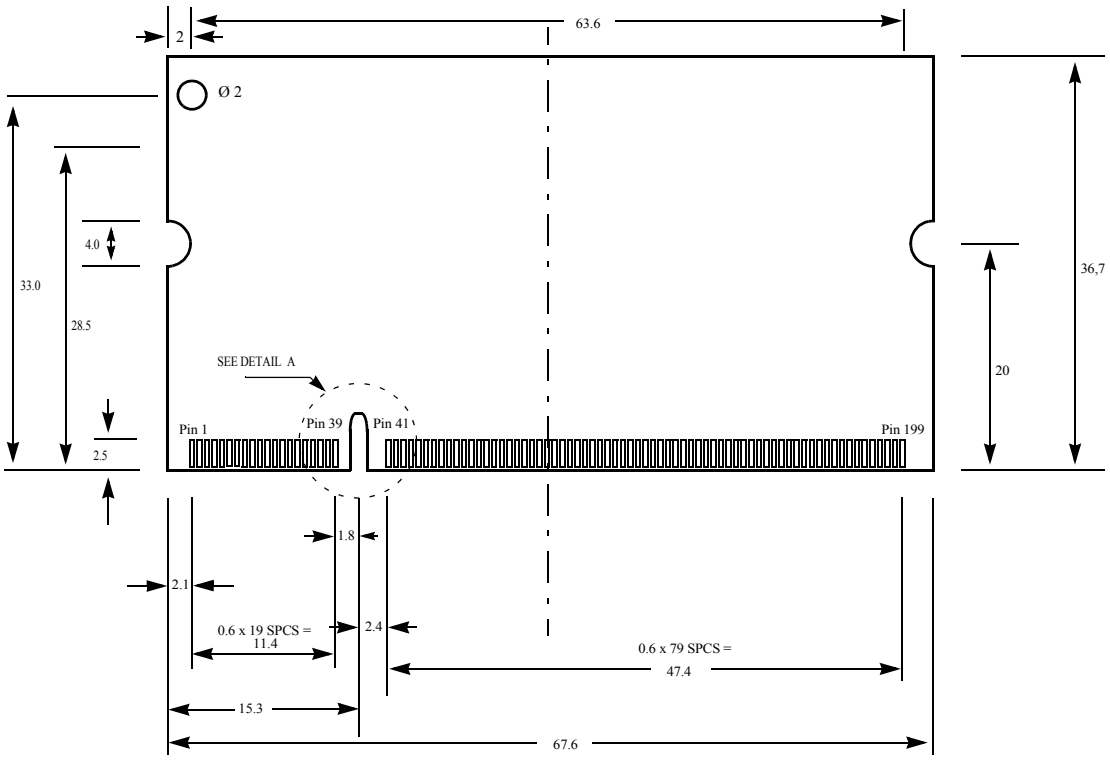


Figure 3. Detail A of Figure 3

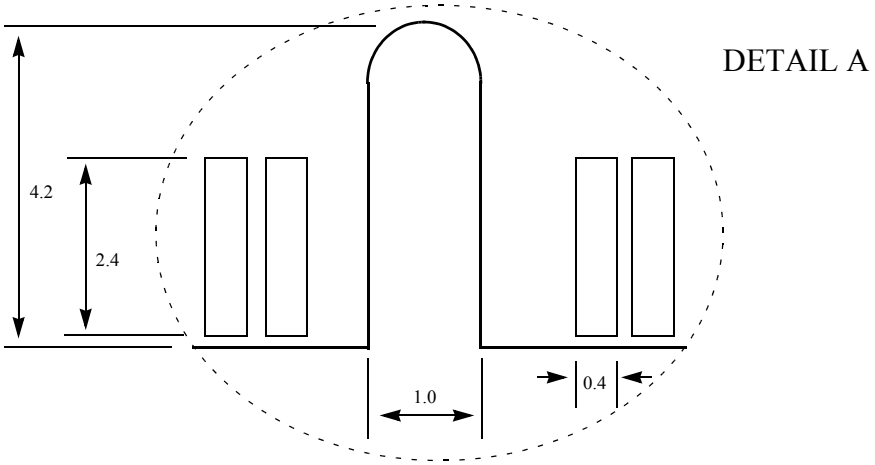
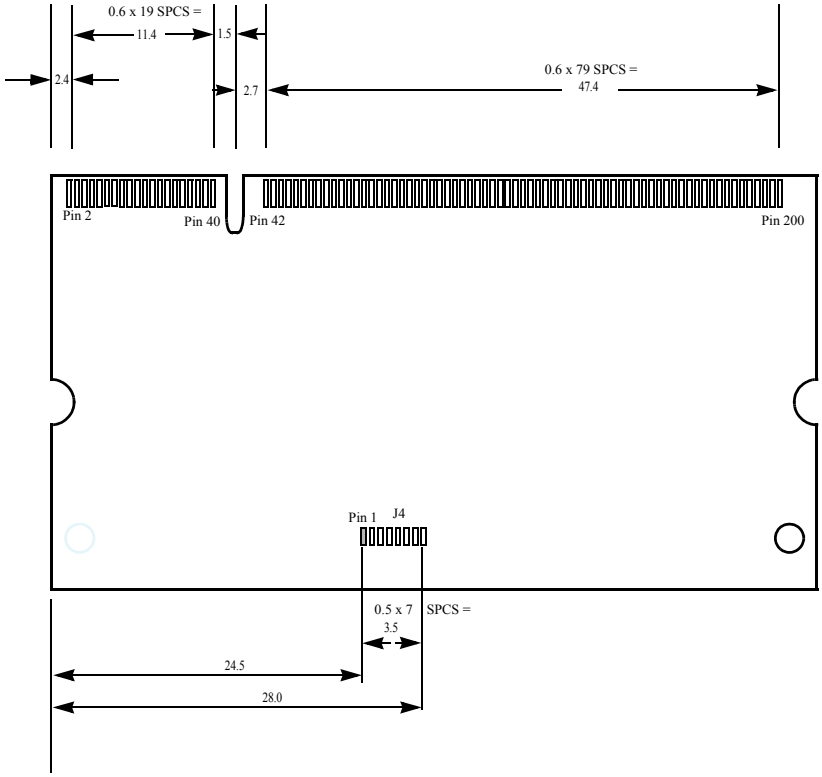


Figure 4. Dimensions of the Trizeps-IV-M Module (bottom view)



The Maximum height is 4.0 mm above the top side and 2.0 mm below the bottom side.

8.0 Revision

Board: Trizeps-IV-M

Revision	PCB number	Date	Changes
1.1		03.05.2010	based on Version 1.3.1 of Trizeps-IV datasheet
1.2		13.02.2013	codec change: UCB1400 --> WM9715L
1.2.1		26.11.2014	Add note for signal HEADPHONE_GND in table 1

9.0 Disclaimer