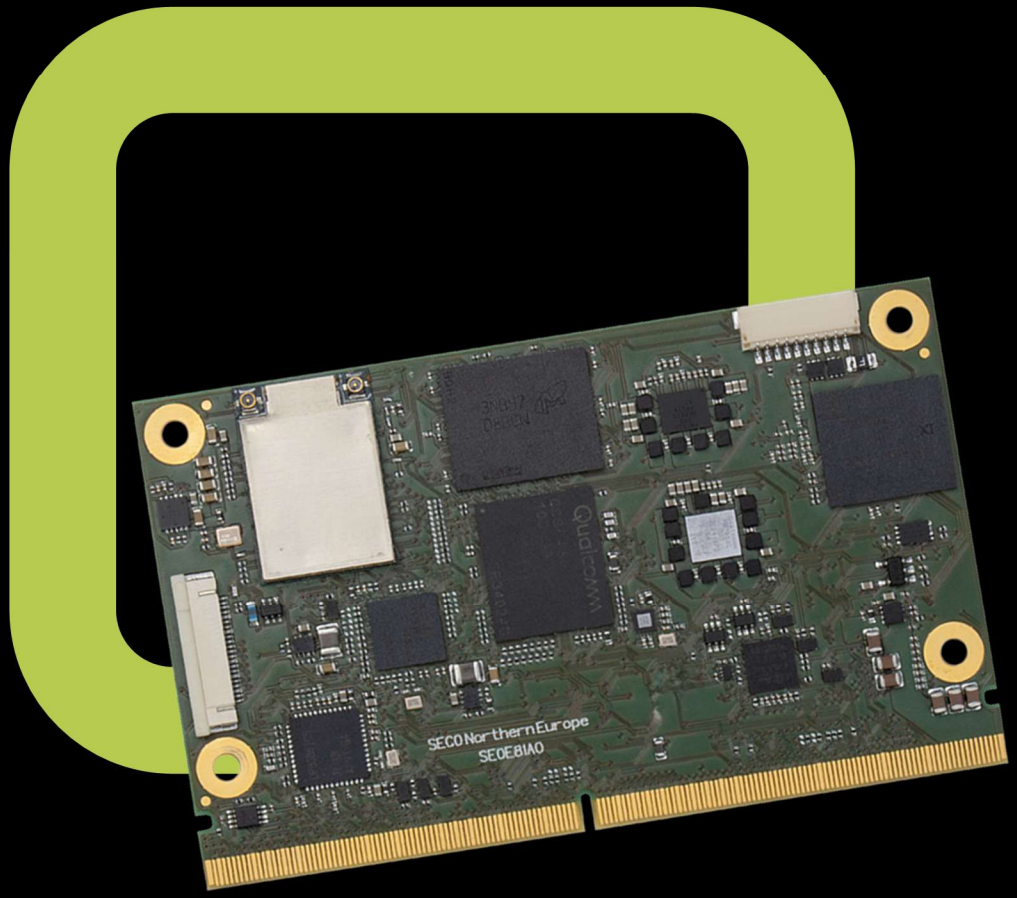
SMARC®

User Manual



SOM-SMARC-QCS

SMARC® Rel. 2.2 compliant module with Qualcomm Dragonwing™ QCS5430 or QCS6490 Applications Processors

SMARC module

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

SECO

REVISION HISTORY

Revision	Date	Note	Rif
1.0	18th March 2025	Draft release	MS
1.1	09th October 2025	Based on REV. C1	MS
1.2	17th December 2025	Added Block diagram in detail, new links included	MS
1.3	27th April 2026	Completed power consumption data	MS
1.4	15th July 2026	Changed Block Diagram to version 1.9 and corrected PCIe description	MS

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Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

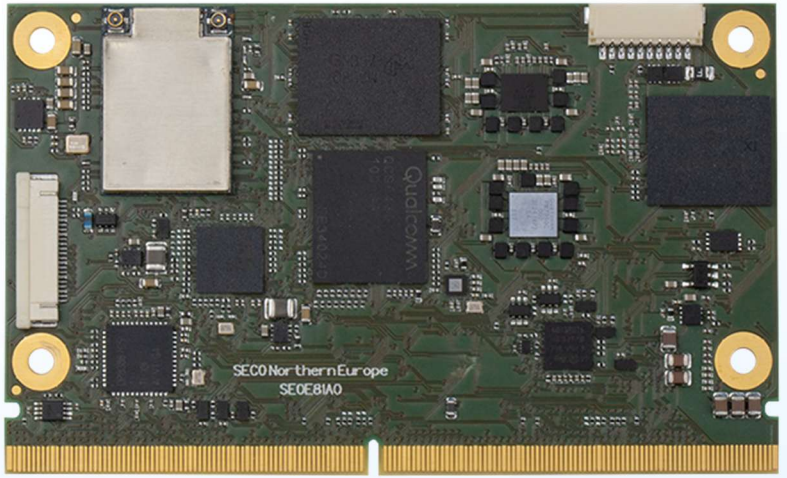
Our team is ready to assist.

INDEX

1.1 Warranty 5
1.2 Information and assistance 6
1.3 RMA number request 6
1.4 Safety 7
1.5 Electrostatic Discharges 7
1.6 RoHS compliance 7
1.7 Safety Policy 8
1.8 Terminology and definitions 9
1.9 Reference specifications 11
Chapter 2. OVERVIEW 13
2.1 Introduction 14
2.2 Technical Specifications 15
2.3 Electrical Specifications 17
2.3.1 Electrical characteristics 17
2.3.2 Power consumption 18
2.3.3 Power Rails meanings 18
2.4 Mechanical Specifications 19
2.5 Supported Operating Systems 19
2.6 Block Diagram 20
Chapter 3. CONNECTORS 21
3.1 Introduction 22
3.2 Connectors description 23
3.2.1 WiFi/BTLE Module 23
3.2.2 SMARC® Connector 24
Chapter 4. Appendices 50
4.1 SoC to Connector Pinout 51
4.2 Thermal Design 58

INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://support.seco.com (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.



Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210
- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request an RMA number, please visit SECO's web-site https://support.seco.com. On the home page, please follow the procedure described.

An RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The SOM-SMARC-QCS5430/6490 module uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!** Always switch the power off, unplug the power supply unit and wait until the unit has cooled down, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.

1.5 Electrostatic Discharges

The SOM-SMARC-QCS module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!** Whenever handling any of these boards, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The SOM-SMARC-QCS module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Policy

In order to meet the safety requirements of IEC 62368-1:2018 standard for Audio/Video, information and communication technology equipment, the SOM-SMARC-QCS Module shall be:

- used exclusively on SMARC 2.1 fully compliant Carrier boards;
- connections from or to the Module have to be compliant to ES1 requirements;
- used inside a fire enclosure made of non-combustible material or V-1 material (the fire enclosure is not necessary if the maximum power supplied to the module never exceeds 100 W, even in worst-case fault);
- used along with CPU Heatspreader/heatsinks designed according to the thermal characteristics indicated in the par. 2.2 and to the mechanical characteristics indicated in par.2.4.

The manufacturer which includes a SOM-SMARC-QCS module in his end-user product shall:

- Install the device inside an enclosure compliant with all applicable IEC 62368-1 requirements;
- Prevent children from accessing the board;
- Prescribe temperature and humidity range for operating, transport and storage conditions;
- verify the compliance with B.2 and B.3 clauses of the IEC 62368-1 standard when the module works in its own final operating condition;
- provide an instructional safeguard against thermal injuries, according to clause 9.5.2 of the above mentioned standard. This instructional safeguard must be placed both on end-user product's User Manual and on the products itself (Danger Label IEC 60417-5041, it must be placed near the CPU or its heatsink);
- When an heatsink with FAN is used, then the FAN should be managed with signals made available by SMARC Card Edge Connector of the SOM-SMARC-QCS module. Its electrical characteristics must be compliant to the requirements of SMARC Rel.2.2 standard.

1.8 Terminology and definitions

API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BTLE	Bluetooth Low Energy, a wireless personal area network technology
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
CSI2 processor	MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
DVI	Digital Visual interface, a type of display video interface
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
LPDDR4	Low-Power Double Data Rate Synchronous Dynamic Random Access Memory, 4th generation
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics

OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port.
PCI-e	Peripheral Component Interface Express
PWM	Pulse Width Modulation
PWR	Power
RGMII	Reduced Gigabit Reduced Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer (PHY)
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
USB	Universal Serial Bus
uSDHC	Ultra Secure Digital Host Controller

1.9 Reference specifications

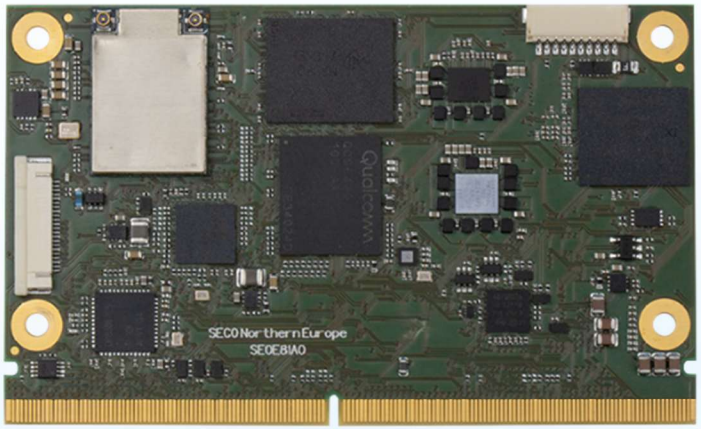
Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
CSI	http://www.mipi.org/specifications/camera-interface
DDC	http://www.vesa.org
Fast Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
Qualcomm QCS6490	https://www.qualcomm.com/products/internet-of-things/qcs6490
Qaulcomm QCS5430	https://www.qualcomm.com/products/internet-of-things/qcs5430
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
SMARC Design Guide 2.0	https://www.sget.org/fileadmin/user_upload/SMARC_DG_V2.pdf
SMARC Hardware Specification 2.1.1	https://sget.org/wp-content/uploads/2020/05/SMARC_V211.pdf
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds

USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
UFS 2.2 and 3.1	https://www.jedec.org/standards-documents/focus/flash/universal-flash-storage-ufs

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Supported Operating Systems
- Block Diagram



2.1 Introduction

SOM-SMARC-QCS5430 /QCS6490 is a SMARC Rel. 2.2 compliant module with Qualcomm Dragonwing™ family Applications Processors. Featuring multicore and real-time processing together with neural networks acceleration and a vision system. It is a scalable solution designed by SECO for home automation, transportation, digital signage and vending machines, and applicable to scenarios requiring advanced security, connectivity, multimedia and real-time response.

The module offers a very high level of integration, both for all most common used peripherals in the ARM domain and for bus interfaces typically used in the x86 domain, like PCI-Express

Presented in the SMARC ("Smart Mobility ARChitecture") form factor, offering the computing abilities of a standard board, with the possibilities of combining with a ready-to-use carrier board like the SECO CSM-B79 or customised carrier board.

For external interfacing to standard devices, a carrier board with a 314-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as the integration of other peripherals/devices not already included in SOM-SMARC-GENIO module.

2.2 Technical Specifications

Processors

Qualcomm Dragonwing™ QCS Family:

QCS5430 (FP1) (Total 6 cores)

Kryo Gold: 2 x CPU subsystem based on A78 at 2.13 GHz

Kryo Silver: 4 x CPU subsystem based on A55 at 1.8 GHz

QCS5430 (FP2) (total 6 cores)

Kryo Prime: 1 x CPU subsystem based on A78 at 2.2 GHz

Kryo Gold: 3 x CPU subsystem based on A78 at 2.13 GHz

Kryo Silver: 4 x CPU subsystem based on A55 at 1.8 GHz

QCS6490 (total 8 cores)

Kryo Prime: 1 CPU subsystem based on A78 at 2.7 GHz

Kryo Gold: 3 x CPU subsystem based on A78 at 2.4 GHz

Kryo Silver : 4 x CPU subsystem based on A55 at 1.9 GHz

Memory

- Soldered-down LPDDR5-6400 memory, up to 12GB total,
- 32-bit interface 2 channels

Graphics

- Integrated Graphics Processing Unit Qualcomm® AdrenoTM 642L (QCS5430)
- Integrated Graphics Processing Unit Qualcomm® AdrenoTM 643L(QCS6490)
- supports 2 independent displays, OpenGL , Open CL , Vulkan. Embedded VPU
- supports H/W decoding of HEVC/H.265, AVC/H.264
- supports H/W encoding of HEVC/H.265, AVC/H.264

Video Interfaces

- LVDS dual channel 18/24 bit, eDP V1.4, MIPI DSI 4 lanes,
- Display Port 1.4 through USB 3.1 Type C

Video Resolution

- Primary display: FHD+ @120 fps
- Secondary display: up to 4k Ultra HD @60Hz

AI-accelerator

- QCS5340: up to 9 INT8 TOPS
- QCS6390: 12.15 INT8 TOPS

Mass Storage

- eMMC 5.1 Drive soldered on-board, up to 64GB
- or /and
- SD 4-bit interface (boot device) opt. UFS 2.x/3.1 flash

PCI Express

- PCIe lanes Gen3: 1 port x1 lane, 1 port x2 lanes (only FP2 and QCS6490)

Networking

- 2x Gigabit Ethernet interfaces
- Opt. Wi-Fi + BT5.0

USB

- 1x USB 3.1 (configurable as 1x USB 2.0 OTG) additional
- 1x USB 2.0 or 4x USB 2.0 (Hub option)

Audio

- 2x I2S Audio interface

Serial ports

- 2 x UART Tx/Rx/RTS/CTS
- 2 x UART Tx/Rx
- 1 x CAN via SPI

Other Interfaces

- 1x 2-Line MIPI CSI ,2x 4-Line MIPI CSI, with ISP support
- 13xGPIO
- 2xPWM
- I2C
- SPI
- Power Management
- Watchdog
- Fan

Power supply voltage: +5V DC (+5V Standby opt)

Ultra Low Power RTC

Operating temperature:

- Commercial version 0°C ÷ +60°C **.
- Industrial version -30°C ÷ +85°C **.

Dimensions: 50 x82 mm (1.97" x 3.23")

Supported Operating Systems:

- CleaOS (Yocto Linux 64-bit)

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated. Please also check paragraph 4.2*

2.3 Electrical Specifications

According to SMARC specifications, the SOM-SMARC-QCS module needs to be supplied only with an external +5V_{DC} power supply.

For Real Time Clock working, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from +5V_{DC} power rail.

2.3.1 Electrical characteristics

Absolute maximum ratings reflect conditions that the module may be exposed outside of the operating limits, without experiencing immediate functional failure. Functional operation is only expected during the conditions indicated under "Recommended Operating Conditions". Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the module. Exposure to absolute -maximum rated conditions for extended periods may affect device reliability.

Absolute maximum ratings

	Pin	Min	Max	Unit
Supply Voltage 5V	5V_SLEEP	-0.3	5.5	V
RTC 3.0V	VDD_RTC	-0.3	3.5	V
Operating Temperature (Commercial)	$T_{Storage}$	0	+60	°C
Operating Temperature (Industrial)	$T_{Storage}$	-30	+85	°C
Storage Temperature	$T_{Storage}$	-40	+85	°C

2.3.2 Power consumption

Test environment: Baseboard B79, 10.1" Display , Ethernet, Mirco-USB ,

Status	QCS5430 (EE81-2131-3537-E3) 4GB RAM, 128GB UFS, LVDS, 2x Ethernet OS: clea-os-embedded__scarthgap_2-03-00	QCS6490 (EE81-3232-5537-E3) 8GB RAM, 128GB UFS, Dual LVDS, 2x Ethernet 1GB OS: clea-os-embedded__scarthgap_2-03-00
	Average	Average
Booting to prompt	3,82W	2,71W (based on shorter time to prompt)
Idle	4,66W	4,74W
GPU and CPU working at full load, video reproduction of 1080p video	6,78W	8,36W

2.3.3 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VDD_IN: Module power input voltage. +5V voltage directly coming from the card edge connector.

VDD_RTC: Low current RTC circuit backup power. 3V coin cell voltage coming from the edge card for supplying the RTC clock on the QCS5430 / QCS6490

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +1.8V_RUN,+3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

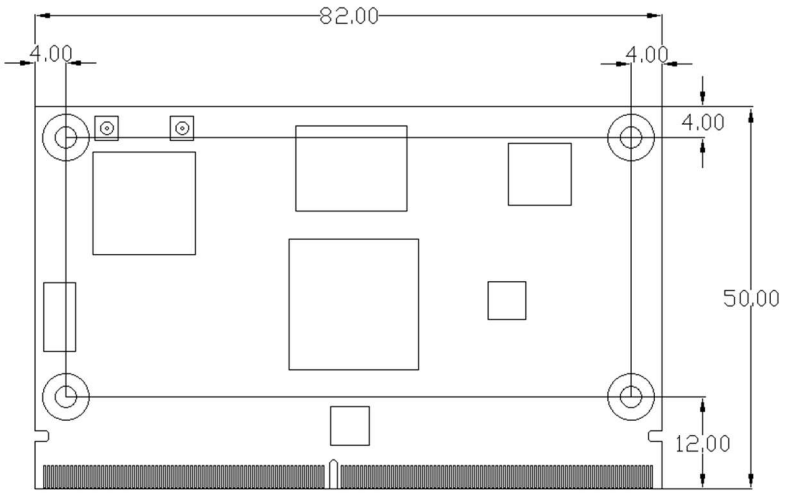
2.4 Mechanical Specifications

According to SMARC® specifications, the board dimensions are: 50 x 82 mm (1.97" x 3.23") including the pin numbering and edge finger pattern.

Printed circuit of the board is made of 12 layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs.

When using different connector heights, please consider that, according to SMARC specifications, components placed on bottom side of the module will have a maximum height of 1.3mm. Keep this value in mind when choosing the MXM connector's height, if there is the need to place components on the carrier board in the zone below the SMARC module.



2.5 Supported Operating Systems

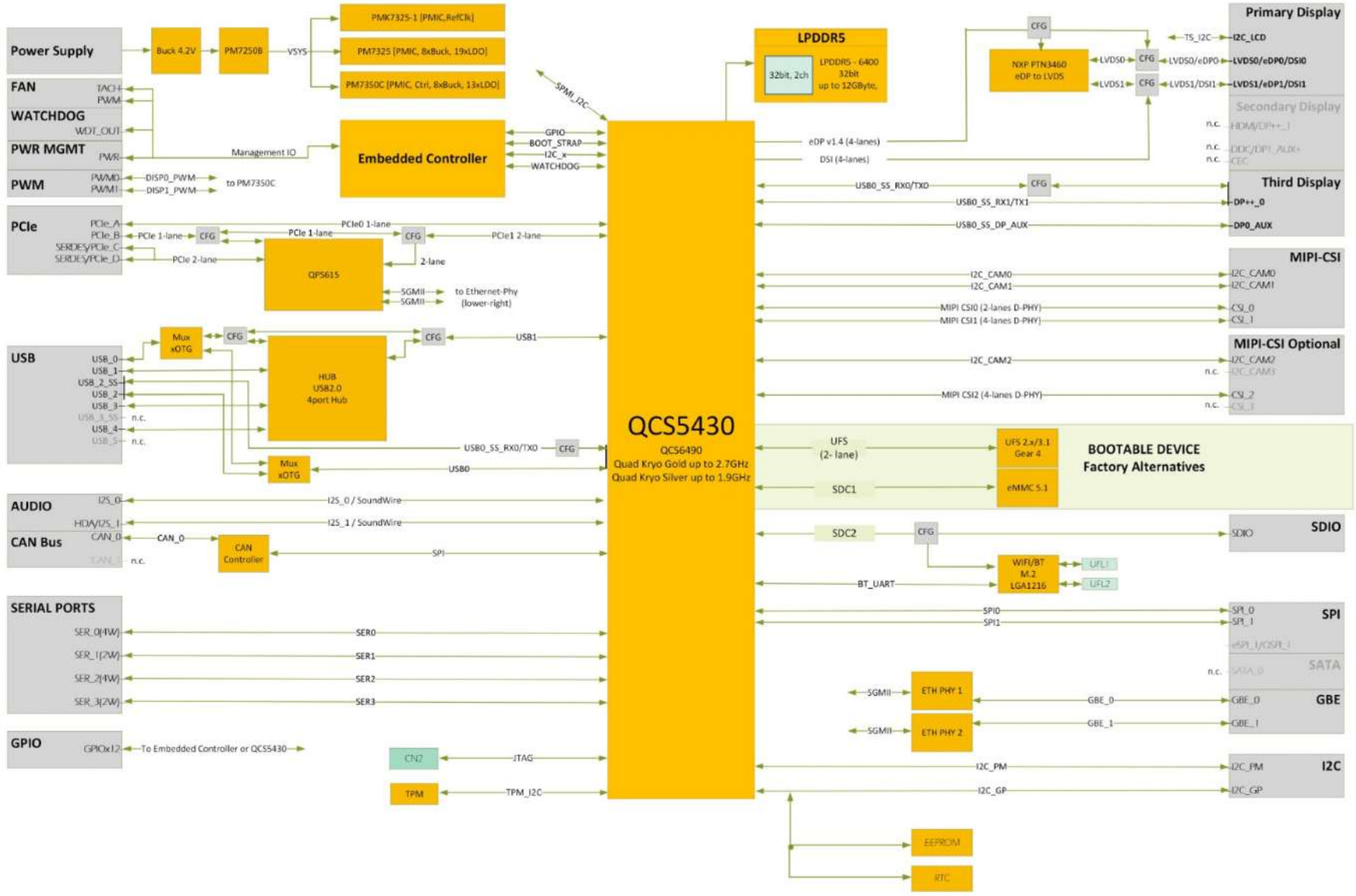
SOM-SMARC-QCS module supports the following operating systems:

- CleaOS (Yocto Linux based)

SECO will offer the BSP (Board Support Package) for these O.Ss, to reduce at minimum SW development of the board, supplying all the drivers and libraries needed for use both with the SMARC board and the Carrier Board, assuming that the Carrier Board is designed following SECO SMARC Design Guide, with the same IC's.

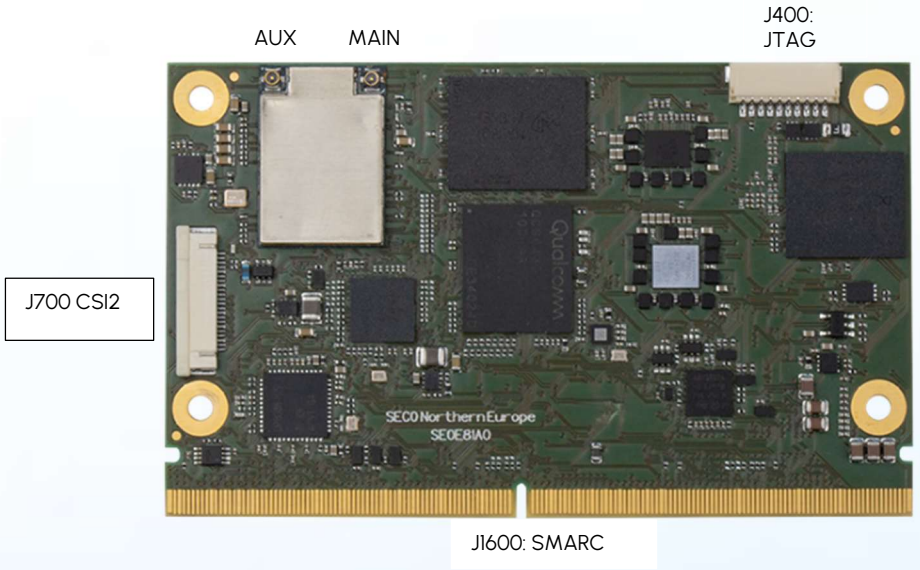
For further details, please visit https://developer.seco.com/clea-os

2.6 Block Diagram



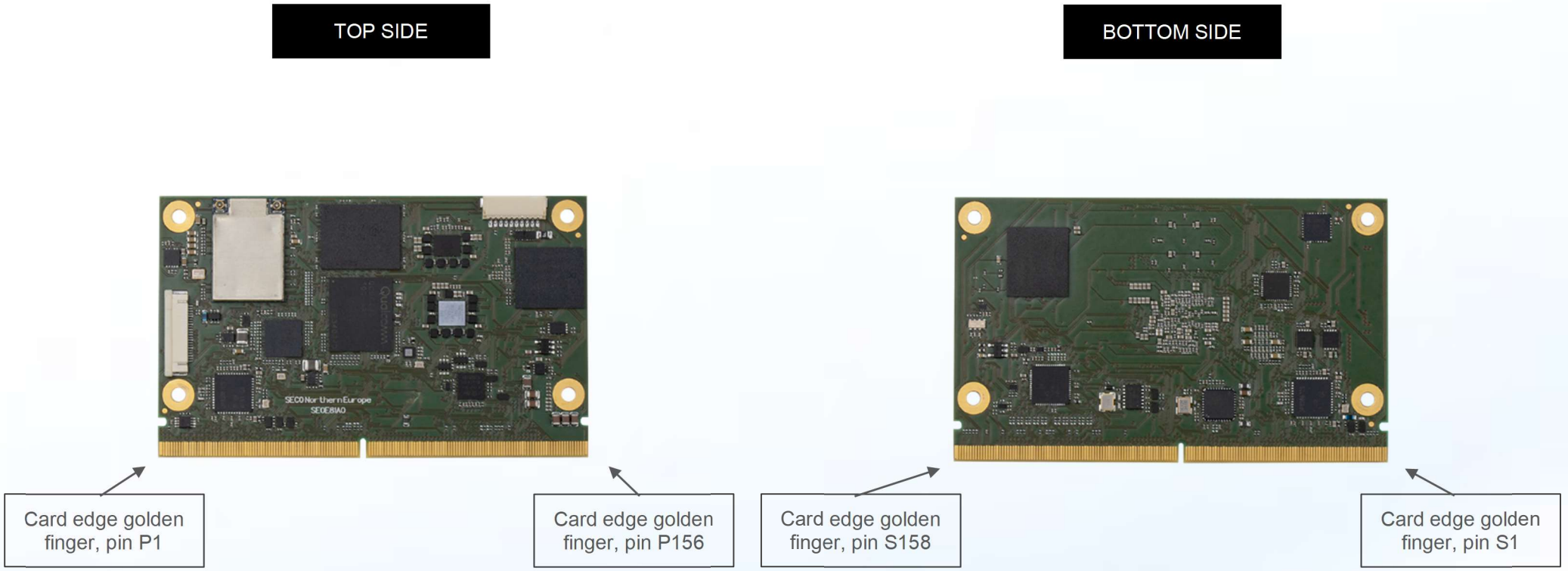
Chapter 3.
CONNECTORS

- Introduction
- Connectors description



3.1 Introduction

According to SMARC specifications, all interfaces to the board are available through a single card edge connector.

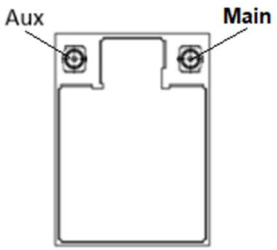


3.2 Connectors description

3.2.1 WiFi/BTLE Module

This SMARC® module can be equipped, by factory option, with a Dual band (2.4GHz + 5.0 GHz) WLAN 802.11 a/b/g/n/ac + BT 5.0 combo embedded module SONA-MT921 or AzureWave AW-CM27NF

Aux antenna is used for WLAN and BT while main antenna is used for WLAN only. These are type IPEX MHF4 RF connectors.



3.2.2 SMARC® Connector

According to SMARC® Rel. 2.2 specification, all interface signals are reported on the card edge connector, which is a 314-pin Card Edge that can be inserted into standard low profile 314 pin 0.5mm right pitch angle connector that was originally defined for use with MXM3 graphics cards.

Not all signals contemplated in the SMARC® Rel. 2.2 are implemented on card edge connector, therefore, please refer to the following table for a list of effective signals reported on the card edge connector.

Consider that the signals labelled as RSVD are for factory production use only and shall be left unused, otherwise the module may not boot or function properly.

For accurate signals description, please consult the following paragraphs.

SMARC® Golden Finger Connector – CN2							
TOP SIDE				BOTTOM SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
				S1	I2C_CAM1_CK	O	CAMERA
MANAGEMENT	I	SMB_ALERT_1V8#	P1	S2	I2C_CAM1_DAT	I/O	CAMERA
		GND	P2	S3	GND		
CAMERA	I	CSI1_CK+	P3	S4	N.C.		
CAMERA	I	CSI1_CK-	P4	S5	I2C_CAM0_CK	O	CAMERA
GBE	I/O	GBE1_SDP	P5	S6	CAM_MCK	O	CAMERA
GBE	I/O	GBE0_SDP	P6	S7	I2C_CAM0_DAT	I/O	CAMERA
CAMERA	I	CSI1_RX0+	P7	S8	CSI0_CK+	I	CAMERA
CAMERA	I	CSI1_RX0-	P8	S9	CSI0_CK-	I	CAMERA
		GND	P9	S10	GND		
CAMERA	I	CSI1_RX1+	P10	S11	CSI0_RX0+	I	CAMERA
CAMERA	I	CSI1_RX1-	P11	S12	CSI0_RX0-	I	CAMERA
		GND	P12	S13	GND		
CAMERA	I	CSI1_RX2+	P13	S14	CSI0_RX1+	I	CAMERA
CAMERA	I	CSI1_RX2-	P14	S15	CSI0_RX1-	I	CAMERA
		GND	P15	S16	GND		

CAMERA	I	CSI1_RX3+	P16	S17	GBE1_MDI0+	I/O	GBE
CAMERA	I	CSI1_RX3-	P17	S18	GBE1_MDI0-	I/O	GBE
		GND	P18	S19	GBE1_LINK100#	O	GBE
GBE	I/O	GBE0_MDI3-	P19	S20	GBE1_MDI1+	I/O	GBE
GBE	I/O	GBE0_MDI3+	P20	S21	GBE1_MDI1-	I/O	GBE
GBE	O	GBE0_LINK100#	P21	S22	GBE1_LINK1000#	O	GBE
GBE	O	GBE0_LINK1000#	P22	S23	GBE1_MDI2+	I/O	GBE
GBE	I/O	GBE0_MDI2-	P23	S24	GBE1_MDI2-	I/O	GBE
GBE	I/O	GBE0_MDI2+	P24	S25	GND		
GBE	O	GBE0_LINK_ACT#	P25	S26	GBE1_MDI3+	I/O	GBE
GBE	I/O	GBE0_MDI1-	P26	S27	GBE1_MDI3-	I/O	GBE
GBE	I/O	GBE0_MDI1+	P27	S28	N.C		
		N.C.	P28	S29	PCIE_D_TX+	O	PCIE
GBE	I/O	GBE0_MDI0-	P29	S30	PCIE_D_TX-	O	PCIE
GBE	I/O	GBE0_MDI0+	P30	S31	GBE1_LINK_ACT#	O	GBE
		N.C.	P31	S32	PCIE_D_RX+	I	PCIE
		GND	P32	S33	PCIE_D_RX-	I	PCIE
SDIO_CARD	I	SDIO_WP	P33	S34	GND		
SDIO_CARD	I/O	SDIO_CMD	P34	S35	USB4+	I/O	USB
SDIO_CARD	I	SDIO_CD#	P35	S36	USB4-	I/O	USB
SDIO_CARD	O	SDIO_CK	P36	S37	N.C.		
SDIO_CARD	O	SDIO_PWR_EN	P37	S38	I2S_MCK	O	AUDIO
		GND	P38	S39	I2S0_LRCK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D0	P39	S40	I2S0_SDOUT	O	AUDIO
SDIO_CARD	I/O	SDIO_D1	P40	S41	I2S0_SDIN	I	AUDIO
SDIO_CARD	I/O	SDIO_D2	P41	S42	I2S0_CK	O	AUDIO
SDIO_CARD	I/O	SDIO_D3	P42	S43	N.C.		
SPI	O	SPI0_CS0#	P43	S44	N.C.		
SPI	O	SPI0_CK	P44	S45	N.C.		

SPI	I	SPI0_DIN	P45	S46	N.C.		
SPI	O	SPI0_DO	P46	S47	GND		
		GND	P47	S48	I2C_GP_SCL	I/O	I2C
		N.C.	P48	S49	I2C_GP_SDA	I/O	I2C
		N.C.	P49	S50	I2S2_LRCK	I/O	AUDIO
		GND	P50	S51	I2S2_SDOUT	O	AUDIO
		N.C.	P51	S52	SW_I2S2_DAT		AUDIO
		N.C.	P52	S53	SW_I2S2_CLK	O	AUDIO
		GND	P53	S54	N.C.		
SPI	O	SPI1_CS0#	P54	S55	USB5_EN_OC#	I/O	USB
		N.C.	P55	S56	N.C.		
SPI	O	SPI1_CK	P56	S57	N.C.		
SPI	I/O	SPI1_DO	P57	S58	N.C.		
SPI	I/O	SPI1_DIN	P58	S59	N.C.		
		GND	P59	S60	N.C.		
USB	I/O	USB0+	P60	S61	GND		
USB	I/O	USB0-	P61	S62	N.C.		
USB	I/O	USB0_EN_OC#	P62	S63	N.C.		
USB	I	USB0_VBUS_DET	P63	S64	GND		
USB	I	USB0_OTG_ID	P64	S65	N.C.		
USB	I/O	USB1+	P65	S66	N.C.		
USB	I/O	USB1-	P66	S67	GND		
USB	I/O	USB1_EN_OC#	P67	S68	USB3+	I/O	USB
		GND	P68	S69	USB3-	I/O	USB
USB	I/O	USB2+	P69	S70	GND		
USB	I/O	USB2-	P70	S71	USB2_SSTX+	O	USB
USB	I/O	CC1_STM32_RST#	P71	S72	USB2_SSTX-	O	USB
STM32	I	STM32_RST	P72	S73	GND		
		CC2	P73	S74	USB2_SSRX+	I	USB

USB	I/O	USB3_EN_OC#	P74	S75	USB2_SSRX-	I	USB
PCIE	O	PCIE_A_RST#	P75	S76	PCIE_B_RST#	O	PCIE
USB	I/O	USB4_EN_OC#	P76	S77	PCIE_C_RST#	O	PCIE
PCIE	I/O	PCIE_B_CKREQ#	P77	S78	PCIE_C_RX+	I	PCIE
PCIE	I/O	PCIE_A_CKREQ#	P78	S79	PCIE_C_RX-	I	PCIE
		GND	P79	S80	GND		
PCIE	O	PCIE_C_REFCLK+	P80	S81	PCIE_C_TX+	O	PCIE
PCIE	O	PCIE_C_REFCLK-	P81	S82	PCIE_C_TX-	O	PCIE
		GND	P82	S83	GND		
PCIE	O	PCIE_A_REFCK+	P83	S84	PCIE_B_REFCLK+	O	PCIE
PCIE	O	PCIE_A_REFCK-	P84	S85	PCIE_B_REFCLK-	O	PCIE
		GND	P85	S86	GND		
PCIE	I	PCIE_A_RX+	P86	S87	PCIE_B_RX+	I	PCIE
PCIE	I	PCIE_A_RX-	P87	S88	PCIE_B_RX-	I	PCIE
		GND	P88	S89	GND		
PCIE	O	PCIE_A_TX+	P89	S90	PCIE_B_TX+	O	PCIE
PCIE	O	PCIE_A_TX-	P90	S91	PCIE_B_TX-	O	PCIE
		GND	P91	S92	GND		
		N.C.	P92	S93	USB0_DP_RX1+	I/O	USB / DP
		N.C.	P93	S94	USB0_DP_RX1-	I/O	USB / DP
		GND	P94	S95	DP0_AUX_SEL		
		N.C.	P95	S96	USB0_DP_TX1+	I/O	USB / DP
		N.C.	P96	S97	USB0_DP_TX1-	I/O	USB / DP
		GND	P97	S98	DP0_HPD_EXT		
		N.C.	P98	S99	USB0_DP_TX0+	I/O	USB / DP
		N.C.	P99	S100	USB0_DP_TX0-	I/O	USB / DP
		GND	P100	S101	GND		
		N.C.	P101	S102	USB0_DP_RX0+	I/O	USB / DP
		N.C.	P102	S103	USB0_DP_RX0-	I/O	USB / DP

		GND	P103	S104	N.C.		
	I	HDMI_HPD	P104	S105	USB0_DP_AUX+		USB / DP
		N.C.	P105	S106	USB0_DP_AUX-		USB / DP
		N.C.	P106	S107	LCD1_BKLT_EN	O	LCD_SUPPORT
		DP1_AUX_SEL	P107	S108	LVDS1_DSI1_CK+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO0 / CAM0_PWR#	P108	S109	LVDS1_DSI1_CK-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO1 / CAM1_PWR#	P109	S110	GND		
GPIO	I/O	GPIO2 / CAM0_RST#	P110	S111	LVDS1_DSI1_TX0+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO3 / CAM1_RST#	P111	S112	LVDS1_DSI1_TX0-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO4	P112	S113	EDP1_HPD_EXT		
GPIO	I/O	GPIO5/PWM_OUT	P113	S114	LVDS1_DSI1_TX1+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO6 /TACHIN	P114	S115	LVDS1_DSI1_TX1-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO7	P115	S116	LCD1_VDD_EN	O	LCD_SUPPORT
GPIO	I/O	GPIO8	P116	S117	LVDS1_DSI1_TX2+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO9	P117	S118	LVDS1_DSI1_TX2-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO10/EXT_ADC0	P118	S119	GND		
GPIO	I/O	GPIO11/EXT_ADC1	P119	S120	LVDS1_DSI1_TX3+	O	PRIMARY_DISPLAY
		GND	P120	S121	LVDS1_DSI1_TX3-	O	PRIMARY_DISPLAY
MANAGEMENT	I/O	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	O	LCD_SUPPORT
MANAGEMENT	I/O	I2C_PM_DAT	P122	S123	GPIO13	I/O	GPIO
BOOT_SEL	I	BOOT_SEL0#	P123	S124	GND		
BOOT_SEL	I	BOOT_SEL1#	P124	S125	LVDS0_EDP0_TX0+	O	PRIMARY_DISPLAY
BOOT_SEL	I	BOOT_SEL2#	P125	S126	LVDS0_EDP0_TX0-	O	PRIMARY_DISPLAY
MANAGEMENT	O	RESET_OUT#	P126	S127	LCD0_BKLT_EN	O	LCD_SUPPORT
MANAGEMENT	I	RESET_IN#	P127	S128	LVDS0_EDP0_TX1+	O	PRIMARY_DISPLAY
MANAGEMENT	I	POWER_BTN#	P128	S129	LVDS0_EDP0_TX1-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_TX	P129	S130	GND		
ASYNC_SERIAL	I	SER0_RX	P130	S131	LVDS0_EDP0_TX2+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_RTS#	P131	S132	LVDS0_EDP0_TX2-	O	PRIMARY_DISPLAY

ASYNC_SERIAL	I	SER0_CTS#	P132	S133	LCD0_VDD_EN	O	LCD_SUPPORT
		GND	P133	S134	LVDS0_CK_EDP_AUX+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER1_TX	P134	S135	LVDS0_CK_EDP_AUX-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER1_RX	P135	S136	GND		
ASYNC_SERIAL	O	SER2_TX	P136	S137	LVDS0_EDP0_TX3+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER2_RX	P137	S138	LVDS0_EDP0_TX3-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER2_RTS#	P138	S139	I2C_LCD_CK	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER2_CTS#	P139	S140	I2C_LCD_DAT	I/O	LCD_SUPPORT
ASYNC_SERIAL	O	SER3_TX	P140	S141	EDP_BKLT_PWM	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER3_RX	P141	S142	GPIO12	I/O	GPIO
		GND	P142	S143	GND		
CAN	O	CAN0_TX	P143	S144	EDP0_HPD	I	PRIMARY_DISPLAY
CAN	I	CAN0_RX	P144	S145	WDT_TIME_OUT#	O	WATCHDOG
		N.C.	P145	S146	PCIE_WAKE#	I	PCI_e
		N.C.	P146	S147	VDD_RTC		
		VDD_IN	P147	S148	LID#	I	MANAGEMENT
		VDD_IN	P148	S149	SLEEP#	I	MANAGEMENT
		VDD_IN	P149	S150	VIN_PWR_BAD#	I	MANAGEMENT
		VDD_IN	P150	S151	CHARGING#	I	MANAGEMENT
		VDD_IN	P151	S152	CHARGER_PRSNT#	I	MANAGEMENT
		VDD_IN	P152	S153	CARRIER_STBY#	O	MANAGEMENT
		VDD_IN	P153	S154	CARRIER_PWR_ON	O	MANAGEMENT
		VDD_IN	P154	S155	FORCE_RECOV#	I	BOOT_SEL
		VDD_IN	P155	S156	BATLOW#	I	MANAGEMENT
		VDD_IN	P156	S157	TEST#	I	MANAGEMENT
				S158	GND		

***REV B (Differences of CN2 to current Version, REV C)**

CN2			
Signal group	**Type**	**Signal**	**PIN nr.**
STM32	I	STM32_RST	P72
		N.C	P73
Audio	I	I2S2_SDIN	S52
Audio	O	I2S2_CK	S53
LCD_SUPPORT	O	LCD0_BKLT_EN	107
LCD_SUPPORT	O	LCD0_VDD_EN	S116
LCD_SUPPORT	O	LCD0_BKLT_PWM	S122
LCD_SUPPORT	O	LCD0_BKLT_PWM	S141

3.2.3 Camera CSI2 (J700) REV B

CSI2 J700			
Signal group	**Type**	**Signal**	**PIN nr.**
		V3V_RUN	1
		V3V_RUN	2

		GND	3
CAMERA	I	CSI2_RX0_P	4
CAMERA	I	CSI2_RX0_N	5
		GND	6
CAMERA	I	CSI2_RX1_P	7
CAMERA	I	CSI2_RX1_N	8
		GND	9
CAMERA	I	CSI2_RX2_P	10
CAMERA	I	CSI2_RX2_N	11
CAMERA	O	CAM2_RST#	12
CAMERA	I	CSI2_RX3_P	13
CAMERA	I	CSI2_RX3_N	14
		GND	15
CAMERA	I	CSI2_CK_P	16
CAMERA	I	CSI2_CK_N	17
		GND	18
CAMERA	O	I2C_CAM2_CK	19
CAMERA	I/O	I2C_CAM2_DAT	20
CAMERA	O	CAM2_PWR#	21
CAMERA	O	CAM2_MCK	22

3.2.3 Camera CSI2 (J700) REV C

CSI2 J700			
Signal group	**Type**	**Signal**	**PIN nr.**
CAMERA	O	CAM2_MCK	1
CAMERA	O	CAM2_PWR#	2
CAMERA	I/O	I2C_CAM2_DAT	3

CAMERA	O	I2C_CAM2_CK	4
		GND	5
CAMERA	I	CSI2_CK_N	6
CAMERA	I	CSI2_CK_P	7
		GND	8
CAMERA	I	CSI2_RX3_N	9
CAMERA	I	CSI2_RX3_P	10
CAMERA	O	CAM2_RST#	11
CAMERA	I	CSI2_RX2_N	12
CAMERA	I	CSI2_RX2_P	13
		GND	14
CAMERA	I	CSI2_RX1_N	15
CAMERA	I	CSI2_RX1_P	16
		GND	17
CAMERA	I	CSI2_RX0_N	18
CAMERA	I	CSI2_RX0_P	19
		GND	20
		V3V_RUN	21
		V3V_RUN	22



All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.p.A. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

3.2.2.1 LCD Display Support Signals

The panel control signals are:

LCD0_VDD_EN: Panel #1 VDD enable signal. Set high to enable. +1.8V_RUN electrical level Output

LCD0_BKLT_EN: Panel #1 Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_RUN electrical level Output.

LCD0_BKLT_PWM: This signal can be used to adjust the Panel #1 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_RUN electrical level Output.

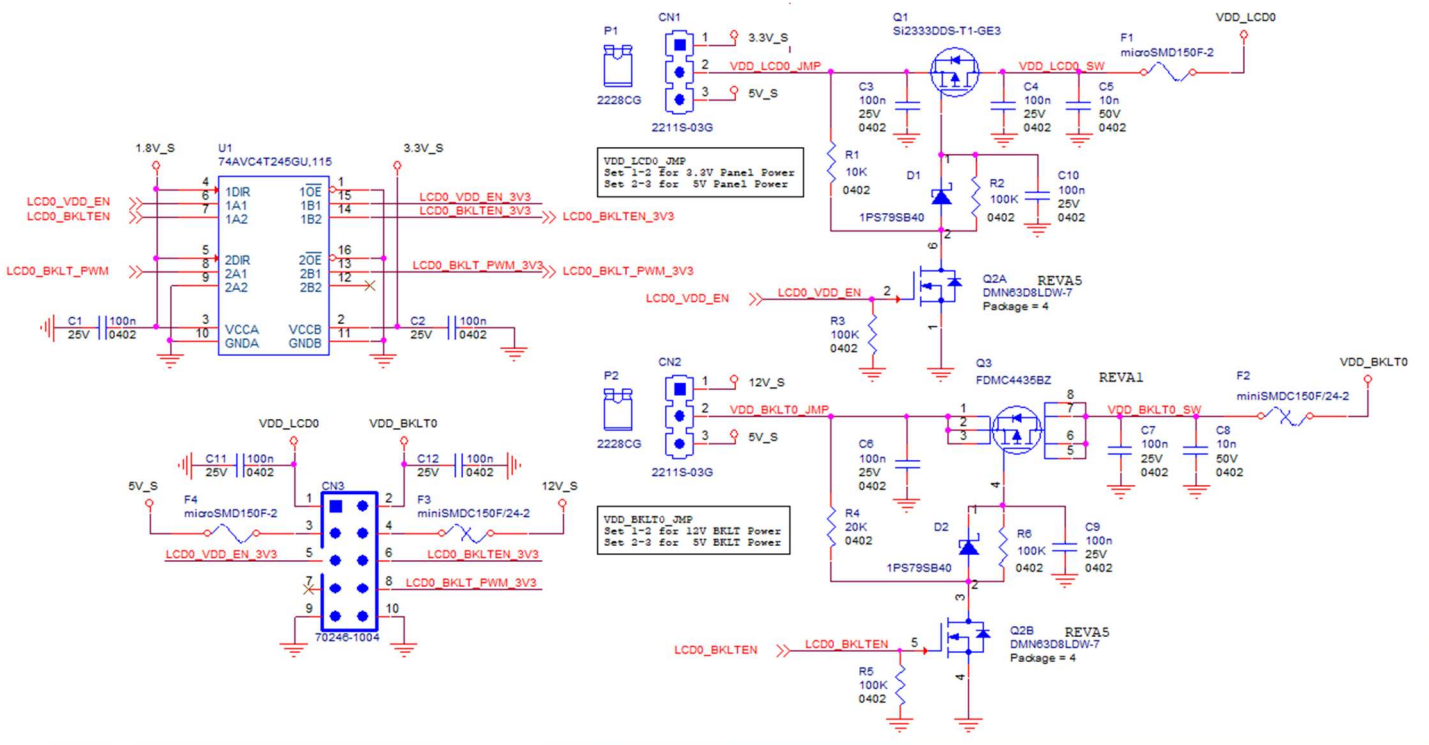
I2C LCD signals are managed by SoC I2C2 bus.

I2C_LCD_DAT: LCD I2C Data. This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level Bidirectional with a 2k2Ω pull-up resistor.

I2C_LCD_CK: LCD I2C Clock: This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level Output with a 2k2Ω pull-up resistor.

On this bus a selection of addresses must be left reserved for on-board peripherals as presented in this table (also consider that this bus is shared with CAM0 from par. 3.2.2.3).

Please refer to the following schematics as an example of connection of LCD display control signals and supply voltage selection jumpers.



3.2.2.2 eDP / Dual Channel LVDS (factory alternatives)

A dual channel LVDS interface is natively supported by the SOC, with a maximum supported resolution of 1920x1200 @ 60Hz, while an eDP interface can be selected as a factory alternative to be present on the edge pinout in place of Channel #0 of the LVDS interface.

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for Channel #0 are LVDS:

LVDS0_0+/LVDS0_0-: LVDS Channel #0 differential data pair #0.

LVDS0_1+/LVDS0_1-: LVDS Channel #0 differential data pair #1.

LVDS0_2+/LVDS0_2-: LVDS Channel #0 differential data pair #2.

LVDS0_3+/LVDS0_3-: LVDS Channel #0 differential data pair #3.

LVDS0_CK+/LVDS0_CK-: LVDS Channel #0 differential Clock.

OR the signals for Channel #0 are eDP :

eDP0_TX0+/ eDP0_TX0-: eDP Channel #0 differential data pair #0.

eDP0_TX1+/ eDP0_TX1-: eDP Channel #0 differential data pair #1.

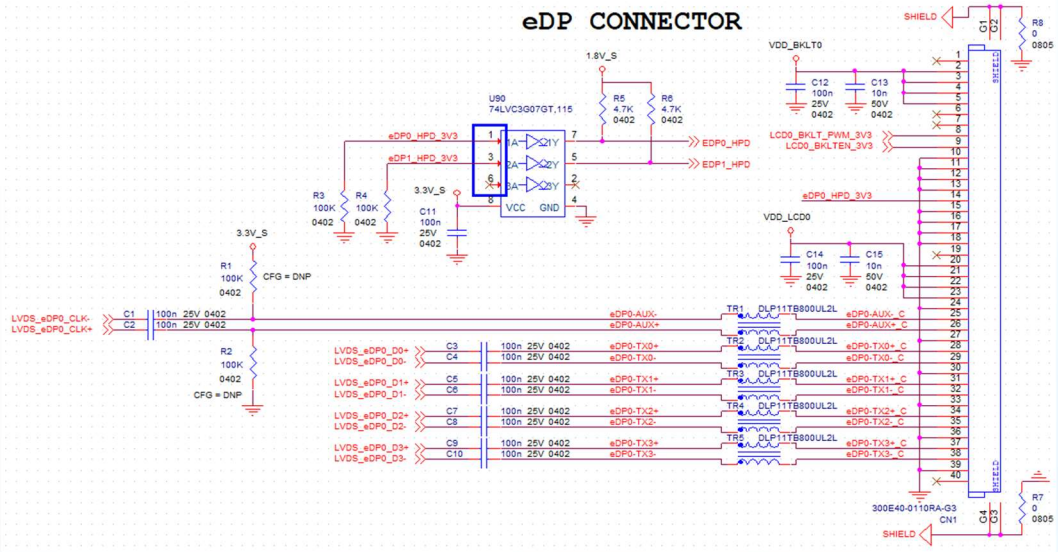
eDP0_TX2+/ eDP0_TX2-: eDP Channel #0 differential data pair #2.

eDP0_TX3+/ eDP0_TX3-: eDP Channel #0 differential data pair #3.

eDP0_AUX+/ eDP0_AUX-: eDP Channel #0 differential Clock.

eDP0_HPD: Hot Plug Detect, Active high Input signal of +1.8V_RUN electrical level from carrier board. 1MΩ pull-down resistor is placed on module for this signal.

Please refer to the following schematics as an example of connection of eDP interface on the carrier board. Hot Plug Detect signal must be buffered to prevent back feeding of power from the display to the module as well as level translation.



The signals for Channel #1 of the LVDS interface is always available on the edge pinout regardless of the factory board configuration.

LVDS1_1+ / LVDS1_0- : LVDS Channel #1 differential data pair #0

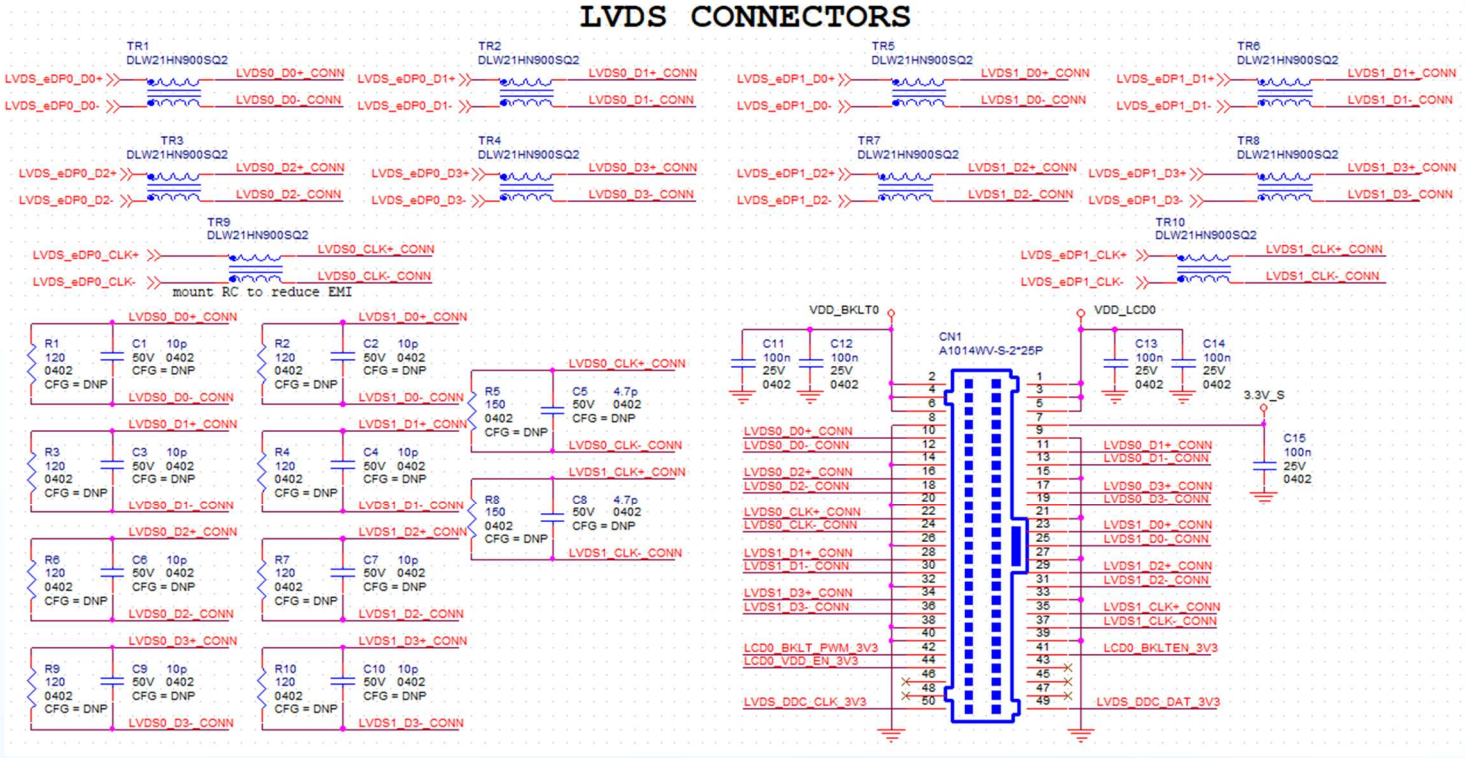
LVDS1_1+/ LVDS1_1-: LVDS Channel #1 differential data pair #1

LVDS1_2+/LVDS1_2-: LVDS Channel #1 differential data pair #2

LVDS1_3+/ LVDS1_3-: LVDS Channel #1 differential data pair #3

LVDS1_CK+/ LVDS1_CK-: LVDS Channel #1 differential Clock

Please refer to the following schematics as an example of connection of dual channel LVDS interface on the carrier board, with EMI filtering section included.



3.2.2.3 Serial Cameras

There are 3 MIPI-CSI interfaces available. The CSI0 interface supports two lanes, the CSI1 and CSI2 interface supports 4 lanes with limited bandwidth.

CSI0_CK+/CSI0_CK-: 2-lane CSI Input Clock Differential Pair
CSI0_RX0+/CSI0_RX0-: 2-lane CSI Input Differential Pair 0
CSI0_RX1+/CSI0_RX1-: 2-lane CSI Input Differential Pair 1

CSI1_CK+/CSI1_CK-: 4-lane CSI Input Clock Differential Pair
CSI1_RX0+/CSI1_RX0- 4-lane CSI Input Differential Pair 0
CSI1_RX1+/CSI1_RX1-: 4-lane CSI Input Differential Pair 1
CSI1_RX2+/CSI1_RX2-: 4-lane CSI Input Differential Pair 2
CSI1_RX3+/CSI1_RX3-: 4-lane CSI Input Differential Pair 3

CSI2_CK+/CSI1_CK-: 4-lane CSI Input Clock Differential Pair
CSI2_RX0+/CSI1_RX0- 4-lane CSI Input Differential Pair 0
CSI2_RX1+/CSI1_RX1-: 4-lane CSI Input Differential Pair 1
CSI2_RX2+/CSI1_RX2-: 4-lane CSI Input Differential Pair 2
CSI2_RX3+/CSI1_RX3-: 4-lane CSI Input Differential Pair 3

CAM_MCK: Master clock Output for CSI Port #0 and/or #1 support, electrical level 1.8V_RUN

CAM2_MCK: Master clock Output for CSI Port #2, electrical level 1.8V_RUN

I2C_CAM0_CK: CSI Port #0 dedicated I2C Bus Clock signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.
I2C_CAM0_DAT: CSI Port #0 dedicated I2C Bus Data signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

I2C_CAM1_CK: CSI Port #1 dedicated I2C Bus Clock signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.
I2C_CAM1_DAT: CSI Port #1 dedicated I2C Bus Data signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

I2C_CAM2_CK: CSI Port #2 dedicated I2C Bus Clock signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.
I2C_CAM2_DAT: CSI Port #2 dedicated I2C Bus Data signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

3.2.2.4 SDI/O interface signals

The Qualcomm Dragonwing QCS5430 / QCS6490 processors offer many different SDIO interfaces, that can be used independently one from the other to implement different mass storages (internal eMMC, internal SD Card, external SDI/O interface).

The SDIO signals of the processor are used for the onboard eMMC storage of the module.

The SDIO signals of the processor are used for the factory optional onboard WiFi/BTLE module.

The SDIO interface of the processor is externally accessible through the edge connector of the module. Supporting 4-bit mode as per the SMARC specification.

The uSDHC controller complies with:

- SD Host Controller Standard Specification version 3.0 with SDR104 signaling to support up to 104MB/sec.
- MMC System Specification version 5.0

The edge accessible SDIO signals are as follows:

SDIO_WP: Write Protect bidirectional signal, electrical level +1.8V_RUN (SDR104) or +3.3V_RUN with 10kΩ pull-up resistor. It is used to communicate the status of Write Protect switch on external SD/MMC card.

SDIO_CMD: Command/Response line. Used to send command from Host (Qualcomm Dragonwing QCS5430 / QCS6490) to the connected card, and to send the response from the card to the Host.

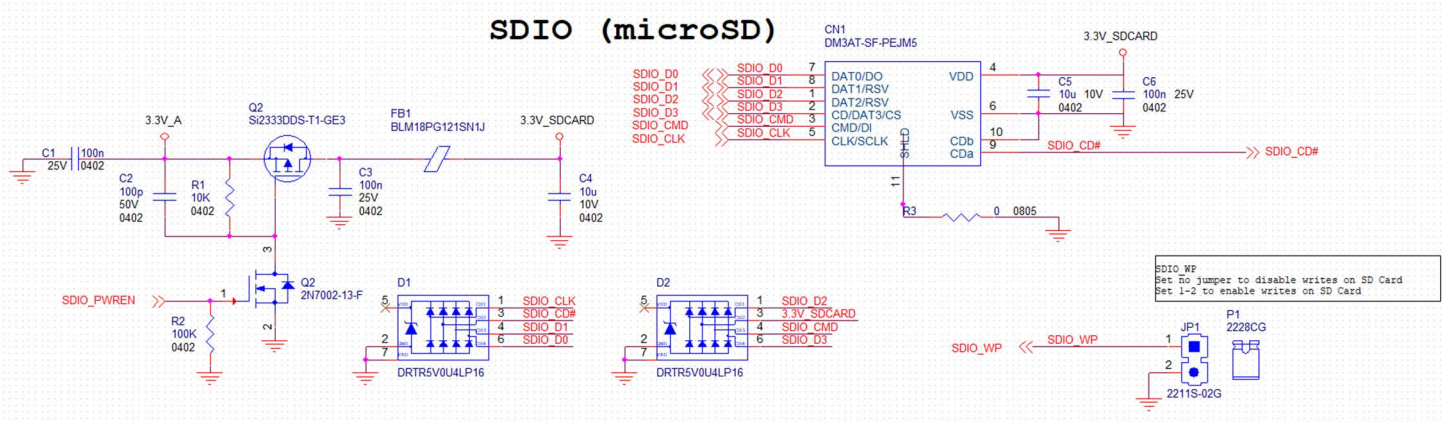
SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +1.8V_RUN (SDR104) or +3.3V_RUN with 10kΩ pull-up resistor. This signal must be externally pulled low to signal that a SDIO/MMC Card is present.

SDIO_CK: Clock Line (output), up to 200MHz maximum frequency for SDR104 Mode (4-bit only).

SDIO_PWR_EN: SDIO Power Enable output, active high signal, electrical level +1.8V_RUN (SDR104) or +3.3V_RUN with 2.2kΩ pull-up resistor. It is used to enable the power line supplying SD/SDIO/MMC devices.

SDIO_[D0÷D3]: SDIO data bus. Signals for 4-bit SD/SDIO/MMC communication mode.

Please refer to the following schematics as an example of connection of SDIO interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression.



3.2.2.5 SPI interface signals

The signals related to SPI0 are as follows:

SPI0_CS0#: SPI primary Chip select, active low output signal. Electrical level +1.8V_RUN.

SPI0_CS1#: SPI secondary Chip select, active low output signal. Electrical level +1.8V_RUN. This signal must be used only in case there are two SPI devices on the carrier board, and the first chip select signal (SPI_CS0#) has already been used. It must not be used in case there is only one SPI device.

SPI0_CK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +1.8V_RUN.

SPI0_DIN: SPI0 Master Data Input, electrical level +1.8V_RUN. Input to QCS5430 / QCS6490 from SPI devices embedded on the Carrier Board.

SPI0_DO: SPI0 Master Data Output, electrical level +1.8V_RUN. Output from QCS5430 / QCS6490 to SPI devices embedded on the Carrier Board.

The signals related to SPI1 are as follows:

SPI1_CS0#: SPI primary Chip select, active low output signal. Electrical level +1.8V_RUN.

SPI1_CK: SPI Master Clock Output. Electrical level +1.8V_RUN. The reference timing signal for all the serial input and output operations.

SPI1_IO_[0:3]: SPI Master Data unidirectional . Electrical level +1.8V_RUN. Data transfer between the master and slaves. In Single I/O mode, SPI_IO_0 is the QSPI master output/QSPI slave input (MOSI) whereas QSPI_IO_1 is the QSPI master input/QSPI slave output (MISO).

SPI interface can support speed up to 20MHz.

3.2.2.6 Audio interface signals

Here are following the signals related to I2S Audio interfaces:

The first I2S interface managed by the SAI2 group of signals of the SoC is always available on the edge pinout:

AUDIO_MCK: Master clock output to Audio codec. Output from the module to the Carrier board, electrical level +1.8V_RUN.

I2S0_LRCK: Left& Right audio synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN.

I2S0_SDOUT: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN.

I2S0_SDIN: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN.

I2S0_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN.

A second I2S interface managed by the SAI3 group of signals of the SoC is available by default on the edge pinout; as a factory alternative can be routed to the BTLE module to support BT Audio.

I2S2_LRCK: Left& Right audio synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN.

I2S2_SDOUT: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN.

I2S2_SDIN: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN.

I2S2_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

Signals routed to the Carrier Board have to be connected to I2S Audio Codecs. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.2.7 I2C Interface

I2C General Purpose signals are managed by SoC I2C5 bus.

I2C_GP_CK: I2C General Purpose clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor

I2C_GP_DAT: I2C General Purpose data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

I2C -Bus Internal	
Address	**Peripheral**
0x6D	PCIe clock buffer
0x50	EEPROM
0x52	RTC

I2C Power Management signals are managed by SoC I2C1 bus.

I2C_PM_CK: Power management clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_ALW with 2.2kΩ pull-up resistor.

I2C_PM_DAT: Power management data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_ALW with 2.2kΩ pull-up resistor

On this bus a selection of addresses must be left reserved for on-board peripherals as presented in this table:

I2C -Bus	
Address	**Peripheral**
0x40	Embedded Controller
0x6D	PCIe clock buffer
0x50	EEPROM
0x52	RTC

3.2.2.8 Asynchronous Serial Ports (UART) interface signals

All UART interface signals are directly managed by the Qualcomm QCS5430 / QCS6490. In all versions, the edge connector offers the four following UART interfaces.

SER0_TX: UART #2 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level.

SER0_RX: UART #2 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor.

SER0_RTS#: UART #2 Interface, Handshake signal, Request to Send (output) line, +1.8V_RUN electrical level.

SER0_CTS#: UART #2 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor.

SER1_TX: UART #4 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level.

SER1_RX: UART #4 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor.

SER2_TX: UART #3 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level.

SER2_RX: UART #3 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor.

SER2_RTS#: UART #3 Interface, Handshake signal, Request to Send (output) line, +1.8V_RUN electrical level.

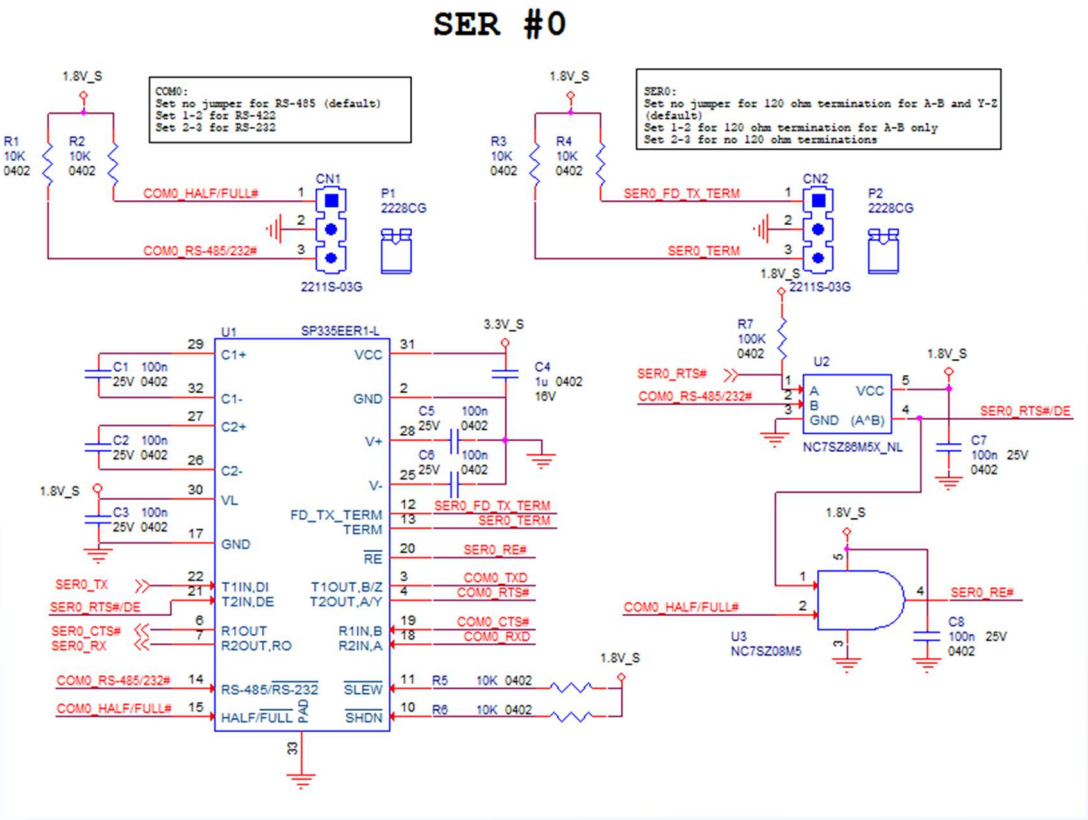
SER2_CTS#: UART #3 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor.

SER3_RX: UART #1 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor.

SER3_TX: UART #1 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level.

Please consider that interface is at +1.8V_RUN electrical level; therefore, please evaluate well the typical scenario of application. If there isn't any explicit need of interfacing directly at +1.8V_RUN level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

In the following schematic here is an example of UART interface on the carrier board, with a multiprotocol transceiver allowing to support RS485/RS-422/RS-232 serial interfaces.



3.2.2.9 USB interface signals

The module has 1x USB 3.1 controller which can be configured at kernel compile time to work as Host or Client and 1x USB ports consisting of 1x USB 2.0 port from the Qualcomm Dragonwing QCS5430 / QCS6490 processor which can be expanded by a MircochipUSB2514 USB 2.0 hub controller to 4 USB 2.0 ports

Here following the signals related to USB interfaces.

USB0+/ USB0-: Universal Serial Bus 2.0 Port #0 differential pair (directly managed by Qualcomm Dragonwing QCS5430 / QCS6490 USB Host Controller core #1).

USB0_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.2 Specification for over current operation information.
The USB0 port is directly managed by Qualcomm Dragonwing QCS5430 / QCS6490 USB Host Controller core #1 and can be used for serial download driving FORCE_RECOV# low.
Please take note that the OTG functionality on this port is not supported at runtime, USB0 must be set to work as Client or Host at kernel compile time.

USB1+/ USB1-: Universal Serial Bus Port 2.0 #1 differential pair.

USB1_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.2 Specification for OC operation information.

USB2+/USB2-: Universal Serial Bus Port 2.0 #2 differential pair.

USB2_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.2 Specification for OC operation information.

USB3+/USB3-: Universal Serial Bus Port 2.0 #3 differential pair.

USB3_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.2 Specification for OC operation information.

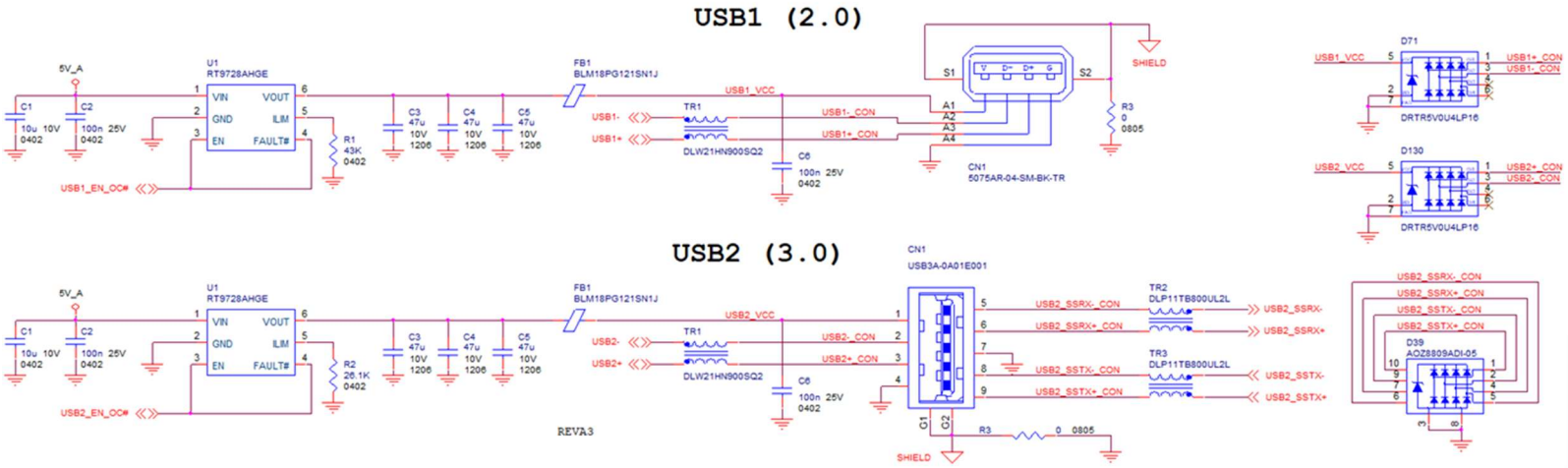
USB4+/USB4-: Universal Serial Bus Port 2.0 #4 differential pair.

USB4_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.2 Specification for OC operation information.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed. Switch with settable current limit on power lines are recommended.

USB2_SSTX+/ USB2_SSTX-: USB 3.0 Port #1 Superspeed Transmit differential pair.

USB2_SSRX+/ USB2_SSRX-: USB 3.0 Port #1 Superspeed Receive differential pair.



3.2.2.10 PCI Express interface signals

The module can offer two PCIe x1 lanes (PCIe_A, PCIe_B) or depending on the configuration 2 PCIe x1 (PCIe_A, PCIe_B) and 1 PCI x2 (PCIe_C & PCIe_D). They are directly managed by Qualcomm QCS5430 / QCS6490 processor (PCI express Gen 3.0 is supported).

Here following the signals involved in PCI express management

PCIE_A_RX+/ PCIE_A_RX-: PCI Express lane #0, Transmitting Output Differential pair.

PCIE_A_TX+/PCIE_A_TX-: PCI Express lane #0, Receiving Input Differential pair.

PCIE_A_REFCK+/ PCIE_A_REFCK-: PCI Express Reference Clock for lane #0, Differential Pair.

PCIE_A_RST#: Reset Signal that is sent from SMARC® Module to a PCI-e device available on the carrier board. Active Low, +3.3V_RUN electrical level.

PCIE_A_CKREQ#: PCIe Port A clock request, can be used for power saving mode on PCIe. Active low, driven by open drain circuitry on the carrier board.

PCIE_WAKE#: PCIe wake up interrupt to host input signal. Active low, +3.3V_ALW electrical level.

3.2.2.11 Gigabit Ethernet signals

Gigabit Ethernet interfaces are realized on the module using two Texas Instruments DP83867CRRGZR Gigabit Ethernet transceivers, which are interfaced to Qualcomm QCS5430 / QCS6490 processor through SGMII interface. and QP615

Here following the signals involved in Gigabit Ethernet #0 management:

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair.

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) Transmit differential pair.

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) Transmit differential pair.

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) Transmit differential pair.

GBE0_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_RUN electrical level.

GBE0_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level.

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_ALW electrical level.

GBE0_SDP: Software defined pin, directly managed by TI Gigabit Ethernet PHY transceiver #0. Bidirectional signal, +3.3V_ALW electrical level.

Here following the signals involved in Gigabit Ethernet #1 management:

GBE1_MDI0+/GBE1_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair.

GBE1_MDI1+/GBE1_MDI1-: Media Dependent Interface (MDI) Transmit differential pair.

GBE1_MDI2+/GBE1_MDI2-: Media Dependent Interface (MDI) Transmit differential pair.

GBE1_MDI3+/GBE1_MDI3-: Media Dependent Interface (MDI) Transmit differential pair.

GBE1_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_ALW electrical level.

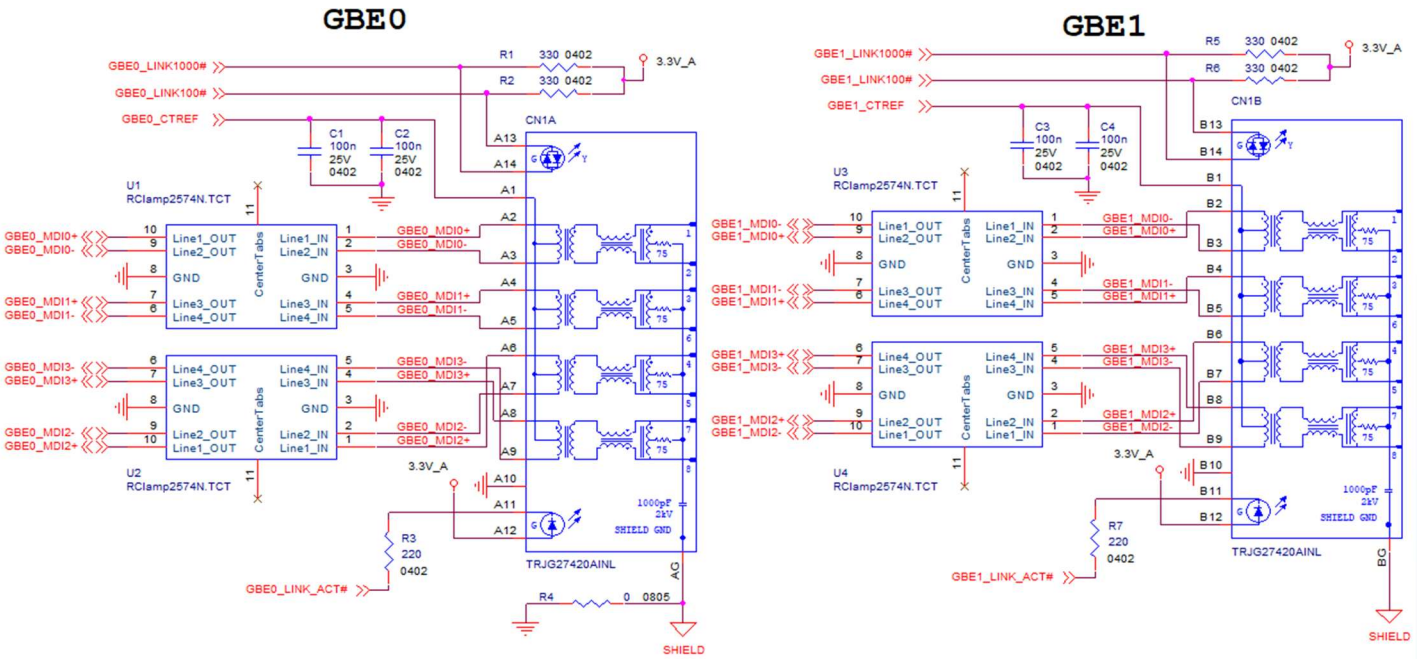
GBE1_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level.

GBE1_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_ALW electrical level.

GBE1_SDP: Software defined pin, directly managed by TI Gigabit Ethernet PHY transceiver #1. Bidirectional signal, +3.3V_ALW electrical level.

Please refer to the following schematics as an example of connection of Ethernet interface on the carrier board, with TVS diodes specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. TI Gigabit Ethernet PHY transceiver, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on SMARC® connector.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary, for both Gigabit Ethernet interfaces



3.2.2.12 CAN interface signals

The CAN interface signals are managed by a MCP2518 SPI to CAN converter.

CAN0_TX: CAN Transmit Output for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal with a 2k2Ω pull-up resistor.

CAN0_RX: CAN Receive Input for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal with a 2k2Ω pull-up resistor.

Please consider that it is not possible to connect the SMARC® CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

3.2.2.13 Watchdog

WDT_TIME_OUT#: Watchdog timer Output. +1.8V_RUN electrical level

3.2.2.14 Miscellaneous signals

GPIO0 / CAM0_PWR#: General Purpose I/O #0, +1.8V_RUN electrical level.
GPIO1 / CAM1_PWR#: General Purpose I/O #1, +1.8V_RUN electrical level.
GPIO2 / CAM0_RST#: General Purpose I/O #2, +1.8V_RUN electrical level.
GPIO3 / CAM1_RST#: General Purpose I/O #3, +1.8V_RUN electrical level.
GPIO4: General Purpose I/O #4, +1.8V_RUN electrical level.
GPIO5 / PWM_OUT: General Purpose I/O #5, +1.8V_RUN electrical level.
GPIO6 / TACHIN: General Purpose I/O #6, +1.8V_RUN electrical level.
GPIO7: General Purpose I/O #7, +1.8V_RUN electrical level.
GPIO8: General Purpose I/O #8, +1.8V_RUN electrical level.
GPIO9: General Purpose I/O #9, +1.8V_RUN electrical level.
GPIO10 /EXT_ADC0: General Purpose I/O #10, +1.8V_RUN electrical level.
GPIO11 /EXT_ADC1: General Purpose I/O #11, +1.8V_RUN electrical level.
GPIO12: General Purpose I/O #12, +1.8V_RUN electrical level.
GPIO13: General Purpose I/O #13, +1.8V_RUN electrical level.

3.2.2.15 Management pins

According to the SMARC® specifications, the input pins listed below are all Active Low, meant to be driven by open drain devices on the carrier board:

VIN_PWR_BAD#: Power Bad indication signal from the Carrier Board.
CARRIER_PWR_ON: Power On. Command to the Carrier Board. Output, +1.8V_ALW electrical level.
CARRIER_STBY#: Stand By command to the Carrier Board. Output, +1.8V_ALW electrical level.
RESET_OUT#: General Purpose Reset. Output, +1.8V_ALW electrical level.
RESET_IN#: General Purpose Reset. Input, +3.3V_ALW electrical level.
POWER_BTN#: Power Button. Input, +3.3V_ALW electrical level.
SLEEP#: Sleep indicator from Carrier board. Input, +3.3V_ALW electrical level (Standby not supported)
LID#: LID Switch. Input, +3.3V_ALW electrical level.

BATLOW#: Battery Low indication signal from the Carrier Board. Input, +3.3V_ALW electrical level.
CHARGING#: Battery Charging Input Signal from the Carrier Board. Input, +3.3V_ALW electrical level.
CHARGER_PRSNT#: Battery Charger Present input from the Carrier Board. Input, +3.3V_ALW electrical level.
TEST#: Held low by Carrier to invoke Module vendor specific test function(s). Input. +3.3V_ALW electrical level with a 10kΩ pull-up resistor.
SMB_ALERT_1V8#: SM Bus Alert# (interrupt) signal. Input, +1.8V_ALW electrical level with a 2k2Ω pull-up resistor.

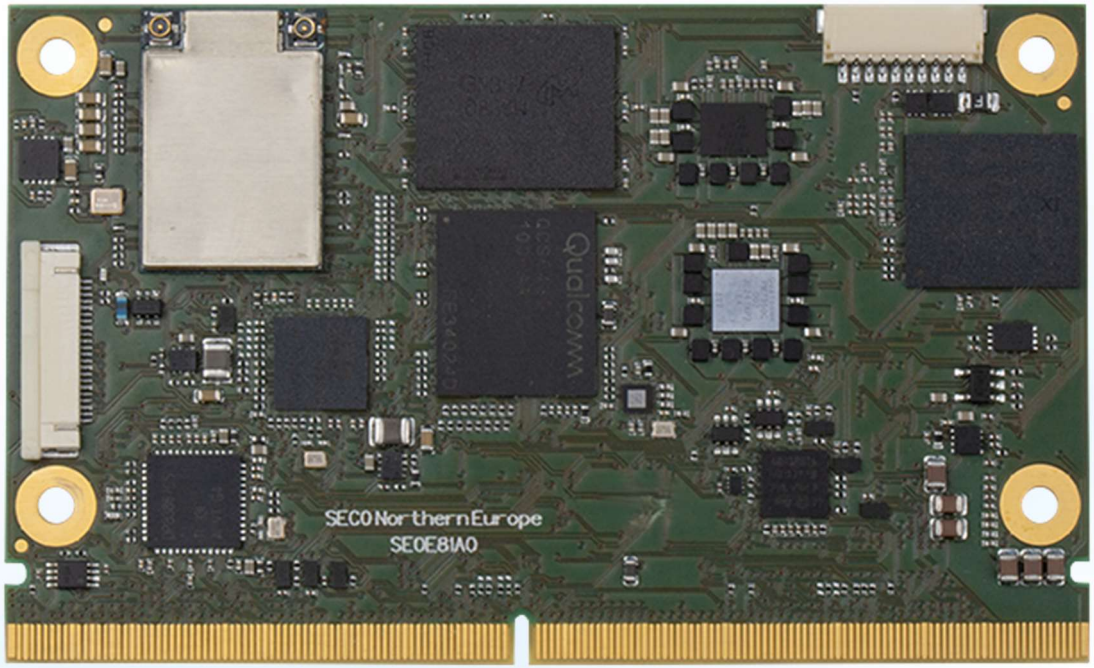
3.2.2.16 Boot Select

The following signals are active low and driven by open drain circuitry on the carrier board.

BOOT_SEL0#: Boot Device Selection #0. Input, +1.8V_ALW electrical level with a 10kΩ pull-up resistor.
BOOT_SEL1#: Boot Device Selection #1. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor.
BOOT_SEL2#: Boot Device Selection #2. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor.
FORCE_RECOV#: Force recovery Mode. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor.

Chapter 4.
Appendices

- SoC to Connector Pinout
- Thermal Design



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4.1 SoC to Connector Pinout

Some of the signals available on the SMARC® Edge Connector can be reprogrammed to implement different functionalities, according to the Genio pin-multiplexing possibilities.
In this table is presented the list of connector signals which are connected to the SoC with the corresponding SoC pad and name. Consult the Genio documentation for the multiplexing capabilities of the listed pads.

SMARC® Golden Finger Connector – CN2 Rev. C0							
TOP SIDE				BOTTOM SIDE			
SoC signal	**SoC pad**	**Pin name**	**Pin nr.**	**Pin nr.**	**Pin name**	**SoC pad**	**SoC signal**
				S1	I2C_CAM1_CK	BB6	GPIO_72
			P1	S2	I2C_CAM1_DAT	BB4	GPIO_71
			P2	S3			
CSI1_NC_CLK_P	AN7	CSI1_CK+	P3	S4			
CSI1_A0_CLK_M	AN5	CSI1_CK-	P4	S5	I2C_CAM0_CK	BB2	GPIO_70
			P5	S6			
			P6	S7	I2C_CAM0_DAT	BC3	GPIO_69
CSI1_B0_LN0_P	AP6	CSI1_RX0+	P7	S8	CSI0_CK_P	AU7	CSI0_NC_CLK_P
CSI1_C0_LN0_M	AP4	CSI1_RX0-	P8	S9	CSI0_CK_N	AU5	CSI0_A0_CLK_M
			P9	S10			
CSI1_A1_LN1_P	AN1	CSI1_RX1+	P10	S11	CSI0_RX0_P	AV6	CSI0_B0_LN0_P
CSI1_B1_LN1_M	AN3	CSI1_RX1-	P11	S12	CSI0_RX0_N	AV4	CSI0_C0_LN0_M
			P12	S13			
CSI1_C1_LN2_P	AR1	CSI1_RX2+	P13	S14	CSI0_RX1_P	AU1	CSI0_A1_LN1_P
CSI1_A2_LN2_M	AR3	CSI1_RX2-	P14	S15	CSI0_RX1-N	AU3	CSI0_B1_LN1_M
			P15	S16			
CSI1_B2_LN3_P	AR5	CSI1_RX3+	P16	S17			

CSI1_C2_LN3_M	AR7	CSI1_RX3-	P17	S18			
			P18	S19			
			P19	S20			
			P20	S21			
			P21	S22			
			P22	S23			
			P23	S24			
			P24	S25			
			P25	S26			
			P26	S27			
			P27	S28			
			P28	S29			
			P29	S30			
			P30	S31			
			P31	S32			
			P32	S33			
GPIO_61	BJ43	SDIO_WP	P33	S34			
SDC1_CMD[SO] SDC2_CMD[WO]	H4 AR41	SDIO_CMD	P34	S35			
GPIO_91	K4	SDIO_CD#	P35	S36			
SDC1_CLK[SO] SDC2_CLK[WO]	G3 AT44	SDIO_CK	P36	S37			
			P37	S38	I2S_MCK	AA45	GPIO_96
			P38	S39	I2S0_LRCK	AH46	GPIO_100
SDC1_DATA0[SO] SDC2_DATA0[WO]	D2 AR43	SDIO_D0	P39	S40	I2S0_SDOUT	AB46	GPIO_99
SDC1_DATA1[SO] SDC2_DATA1[WO]	H2 AR45	SDIO_D1	P40	S41	I2S0_SDIN	AB44	GPIO_98
SDC1_DATA2[SO]	E3	SDIO_D2	P41	S42	I2S0_CK	AA47	GPIO_97

SDC2_DATA2[WO]	AT46						
SDC1_DATA3[SO] SDC2_DATA3[WO]	C3 AT42	SDIO_D3	P42	S43			
GPIO_39	BH44	SPI0_CS0#	P43	S44			
GPIO_38	BH46	SPI0_CK	P44	S45			
GPIO_36	BF42	SPI0_DIN	P45	S46			
GPIO_37	BG43	SPI0_DO	P46	S47			
			P47	S48	I2C_GP_SCL	BN3	GPIO_5
			P48	S49	I2C_GP_SDA	BP2	GPIO_4
			P49	S50	I2S2_LRCK	AV44	GPIO_103
			P50	S51	I2S2_SDOUT	AW47	GPIO_104
			P51	S52	I2S2_SDIN	AV46	GPIO_102
			P52	S53	I2S2_CK	AU45	GPIO_101
			P53	S54			
GPIO_15	L1	SPI1_CS0#	P54	S55			
			P55	S56			
GPIO_14	L3	SPI1_CK	P56	S57			
GPIO_13	M4	SPI1_DO	P57	S58			
GPIO_12	M2	SPI1_DIN	P58	S59			
			P59	S60			
			P60	S61			
			P61	S62			
			P62	S63			
			P63	S64			
			P64	S65			
			P65	S66			
			P66	S67			
			P67	S68			
			P68	S69			

			P69	S70			
			P70	S71	USB2_SS_TX+	BN33	USB0_SS_TX0_P[BO]
			P71	S72	USB2_SS_TX-	BK32	USB0_SS_TX0_M[BO]
			P72	S73			
			P73	S74	USB2_SS_RX+	BM34	USB0_SS_RX0_P[BO]
			P74	S75	USB2_SS_RX-	BK34	USB0_SS_RX0_M[BO]
			P75	S76			
			P76	S77			
			P77	S78			
			P78	S79			
			P79	S80			
			P80	S81			
			P81	S82			
			P82	S83			
PCIE0_REFCLK_P	R3	PCIE_A_REFCLK+	P83	S84			
PCIE0_REFCLK_M	T2	PCIE_A_REFCLK-	P84	S85			
			P85	S86			
PCIE0_RX_P	U1	PCIE_A_RX+	P86	S87			
PCIE0_RX_M	U3	PCIE_A_RX-	P87	S88			
			P88	S89			
PCIE0_TX_P	V4	PCIE_A_TX+	P89	S90			
PCIE0_TX_M	V2	PCIE_A_TX-	P90	S91			
			P91	S92			
			P92	S93	USB0_DP_RX1+	BJ31	USB0_SS_RX1_P
			P93	S94	USB0_DP_RX1-	BL31	USB0_SS_RX1_M
			P94	S95			
			P95	S96	USB0_DP_TX1+	BM32	USB0_SS_TX1_P
			P96	S97	USB0_DP_TX1-	BK32	USB0_SS_TX1_M
			P97	S98	DP0_HPD	BC43	GPIO47

			P98	S99	USB0_DP_TX0+	BN33	USB0_SS_TX0_P[B1]
			P99	S100	USB0_DP_TX0-	BK32	USB0_SS_TX0_M[B1]
			P100	S101			
			P101	S102	USB0_DP_RX0+	BM34	USB0_SS_RX0_P[B1]
			P102	S103	USB0_DP_RX0-	BK34	USB0_SS_RX0_M[B1]
			P103	S104			
			P104	S105	USB0_DP_AUX+	BK30	USB0_DP_AUX_P
			P105	S106	USB0_DP_AUX-	BM30	USB0_DP_AUX_M
			P106	S107			
			P107	S108			
GPIO_18	N1	GPIO0/CAM0_PWR#	P108	S109			
GPIO_19	N3	GPIO1//CAM1_PWR#	P109	S110			
GPIO_20	BG5	GPIO2//CAM0_RST#	P110	S111			
GPIO_21	BG3	GPIO3//CAM1_RST#	P111	S112			
			P112	S113			
			P113	S114			
			P114	S115			
			P115	S116			
			P116	S117			
			P117	S118			
			P118	S119			
			P119	S120			
			P120	S121			
GPIO_9	BK2	I2C_PM_CK	P121	S122			
GPIO_8	BK4	I2C_PM_DAT	P122	S123			
			P123	S124			
			P124	S125			
			P125	S126			
			P126	S127			

			P127	S128			
			P128	S129			
GPIO_26	BE3	SER0_TX	P129	S130			
GPIO_27	BD2	SER0_RX	P130	S131			
GPIO_25	BE1	SER0_RTS#	P131	S132			
GPIO_24	BF2	SER0_CTS#	P132	S133			
			P133	S134			
GPIO_22	BF6	SER1_TX	P134	S135			
GPIO_23	BF4	SER1_RX	P135	S136			
GPIO_58	BG47	SER2_TX	P136	S137			
GPIO_59	BG45	SER2_RX	P137	S138			
GPIO_57	BF44	SER2_RTS#	P138	S139	I2C_LCD_CK	BE45	GPIO_53
GPIO_56	BF46	SER2_CTS#	P139	S140	I2C_LCD_DAT	BD44	GPIO_52
GPIO_62	BJ45	SER3_TX	P140	S141			
GPIO_63	BK46	SER3_RX	P141	S142			
			P142	S143			
			P143	S144			
			P144	S145			
			P145	S146	PCIE_WAKE#	BJ9	GPIO_89
			P146	S147			
			P147	S148			
			P148	S149			
			P149	S150			
			P150	S151			
			P151	S152			
			P152	S153			
			P153	S154			
			P154	S155			
			P155	S156			

P156	S157
	S158

B0 = DP 2-lane
B1 = DP 4-lane
S0 = no eMMC
W0 = no WiFi

4.2 Thermal Design

Highly integrated modules like SOM-SMARC-QCS offer very high performance within small dimensions. On the other hand, the miniaturization of ICs and the high operating frequencies of the processors lead to high heat generation that must be dissipated in order to maintain the CPU within its allowed temperature range.

The operating temperature specified in the Technical Features of SOM-SMARC-QCS module indicates the temperature range in which any and all parts of the heat spreader / heat sink must remain, in order for SECO to guarantee functionality. Hence, these numbers do not necessarily indicate the suitable environmental temperature.

The heat spreader is not intended to be a guaranteed standalone cooling system, but should be used only as a supplemental means of transferring heat to another dissipation system (i.e. heat sinks, fans, heat pipes etc).

It is the customer's responsibility to design and apply an application-dependent cooling system, capable of ensuring that the heat spreader / heat sink temperature remain within the indicated range of the module.

It is an absolute requirement that the customer, after thorough evaluation of the processor's workload in the actual system application, the system enclosure and consequent air flow/Thermal analysis, accurately study and develop a suitable cooling solution for the assembled system.

SECO can provide SOM-SMARC-QCS module specific heat spreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
DM02-00005A	**SMARC® HEAT SPREADER: Heat Spreader SOM-SMARCs QCS(PASSIVE) - Packaged**
DT01-00007A	**Thermal Gap Filler: Thermal Gap Filler 1,5mm 5W/mK**



Warning!

The thermal solutions available with SECO boards are tested in the commercial temperature range (0-60°C), without housing and inside climatic chamber. Therefore, the customer is suggested to study, develop and validate the cooling solution for his system, considering ambient temperature, processor's workload, utilisation scenarios, enclosures, air flow and so on.

In particular, the heat spreader is not intended to be a cooling system by itself, but only as the standard means for transferring heat to cooler, like heatsinks, cold plate, heat pipes and so on.



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