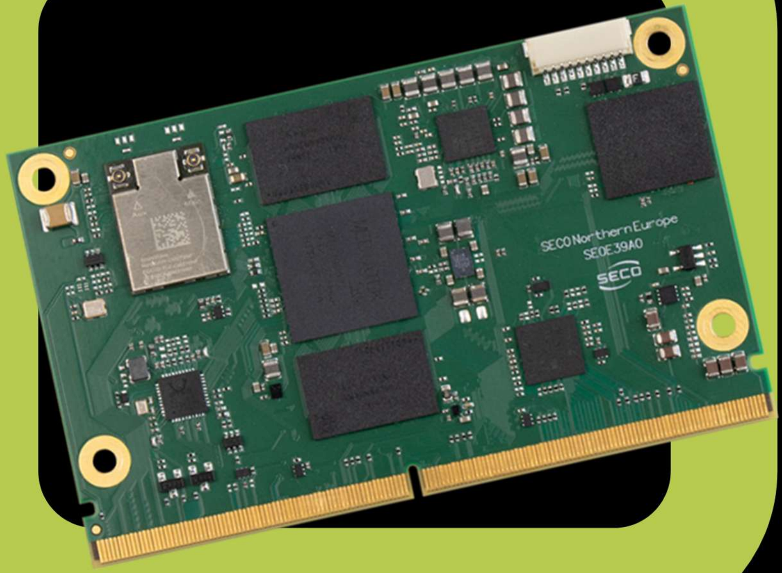
SMARC®

User Manual



SOM-SMARC-Genio 510/700

(E58)

SMARC® Rel. 2.1.1 compliant module with MediaTek Genio 700 or MediaTek Genio 510 Applications Processors

REVISION HISTORY

Revision	Date	Note	Rif
1.0	6th December 2024	First official release	MS
1.1	4th April 2025	Updated 4.2 Thermal Design	MS
1.2	12th September 2025	Updated to REV. C added Chapter 4.3 (Rev.A/B)	MS

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Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

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- Warranty and RMA
- Information and assistance
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1.1 Warranty and RMA

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

To request a RMA number, please visit SECO's web-site. On the home page, please select "Online RMA" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

The authorisation is released after completing the specific ticketing procedure https://support.seco.com/ (Help Topic: Return Merchandise Authorization). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

To open a new account for RMA write to web.rma@seco.com .

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

SECO offers Engineering Samples for early evaluation and development. Engineering Samples are sold "as-is" with no warranty of any kind, neither explicit nor implied.

Here https://www.seco.com/it/EngineeringSamplesPolicy is defined the framework of SECO and customer responsibilities regarding Engineering Samples.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty.

1.2 Information and assistance

What do I have to do if I need assistance?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: place a ticket in the support portal https://support.seco.com/ (Help Topic: HW/SW Support Request).

Note: Please provide the following information when placing a support request on the ticketing portal:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact transcript of every error message encountered.

1.3 Safety

The SOM-SMARC-GENIO module uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!**
>
> Always switch the power off, unplug the power supply unit and wait until the unit has cooled down, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.

1.4 Electrostatic Discharges

The SOM-SMARC-GENIO module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!**
>
> Whenever handling any of these boards, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.5 RoHS compliance

The SOM-SMARC-GENIO module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.6 Safety Policy

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, this product shall be:

- used exclusively on SMARC 2.1.1 fully compliant Carrier boards;
- used inside a fire enclosure made of non-combustible material or V-1 material (the fire enclosure is not necessary if the maximum power supplied to the module never exceeds 100 W, even in worst-case fault);
- used inside an enclosure (the enclosure is not necessary if the temperature of the parts likely to be touched never exceeds 70 °C);
- installed inside an enclosure compliant with all applicable IEC 62368-1 requirements;

The manufacturer which includes this product in his end-user product shall:

- verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition;
- Prescribe temperature and humidity range for operating, transport and storage conditions;
- Prescribe to perform maintenance on the module only when it is off and has already cooled down;
- Prescribe that the connections from or to the Module have to be compliant to ES1 requirements;
- The module in its enclosure must be evaluated for temperature and airflow considerations;
- Install in a way that prevents the access to the board from children;
- Use along with CPU heatspreader/heatsinks designed according to the thermal and mechanical characteristics.
- Verify compliance with chapter 8 of EN62368-1 for mechanical testing based on final product installation
- Verify compliance with chapter Annex V of EN62368-1 for determination of accessible parts based on final product installation
- Prescribe safeguard instructions for parts and surfaces classified as TS3 on final product installation
- When an heatsink with FAN is used, then the FAN should be managed with signals made available by the module from the SMARC Card Edge Connector. Its electrical characteristics must be compliant to the requirements of SMARC Rel.2.1.1 standard.

1.7 Terminology and definitions

API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BTLE	Bluetooth Low Energy, a wireless personal area network technology
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
CSI2	MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host processor
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
DVI	Digital Visual interface, a type of display video interface
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
LPDDR4	Low-Power Double Data Rate Synchronous Dynamic Random Access Memory, 4th generation
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics

OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port.
PCI-e	Peripheral Component Interface Express
PWM	Pulse Width Modulation
PWR	Power
RGMII	Reduced Gigabit Reduced Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer (PHY)
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
USB	Universal Serial Bus
uSDHC	Ultra Secure Digital Host Controller

1.7.1 Trademark Notice

The terms HDMI, HDMI High-Definition Multimedia Interface, and the HDMI Logo are trademarks or registered trademarks of HDMI Licensing Administrator, Inc.

1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
CSI	http://www.mipi.org/specifications/camera-interface
DDC	http://www.vesa.org
Fast Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
SMARC Design Guide 2.0	https://www.sget.org/fileadmin/user_upload/SMARC_DG_V2.pdf
SMARC HW Spec. 2.1.1	https://sget.org/wp-content/uploads/2020/05/SMARC_V211.pdf
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
MediaTek Genio 700	https://www.mediatek.com/products/iot/genio-iot/genio-700
MediaTek Genio 510	https://www.mediatek.com/products/iot/genio-iot/genio-510

Chapter 2.

OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram

2.1 Introduction

SOM-SMARC-GENIO is a SMARC Rel. 2.1.1 compliant module with MediaTek GENIO family Applications Processors. Featuring multicore and real-time processing together with neural networks acceleration and a vision system. It is a scalable solution designed by SECO for home automation, transportation, digital signage and vending machines, and applicable to scenarios requiring advanced security, connectivity, multimedia and real-time response.

The module offers a very high level of integration, both for all most common used peripherals in the ARM domain and for bus interfaces typically used in the x86 domain, like PCI-Express

Presented in the SMARC ("Smart Mobility ARChitecture") form factor, offering the computing abilities of a standard board, with the possibilities of combining with a ready-to-use carrier board like the SECO CSM-B79 or customised carrier board.

For external interfacing to standard devices, a carrier board with a 314-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as the integration of other peripherals/devices not already included in SOM-SMARC-GENIO module.

2.2 Technical Specifications

Processors

MediaTek Genio Family:
- MediaTek Genio 700 ARM® Octa-core CPU (Dual Cortex-A78 @ 2.2 GHz and Six Cortex-A55 @ 2.0 GHz)
- MediaTek Genio 510 ARM® Six-core CPU (Dual Cortex-A78 @ 2.0 GHz and Four Cortex-A55 @ 2.0 GHz)

Memory

Soldered Down LPDDR4X-4000 memory, 32-bit interface, up to 8GB

Graphics

Integrated Graphics Processing Unit Arm Mali-G57 MC3
- supports 2 independent displays, OpenGL , Open CL , Vulkan.

Embedded VPU
- supports H/W decoding of HEVC/H.265, AVC/H.264
- supports H/W ecoding of HEVC/H.265, AVC/H.264

Video Interfaces

1 x HDMI or DP (factory alternatives) up to 4K60
1 x LVDS Dual Channel or eDP (factory alternatives) up to 2560x1600p60

Video Resolution

HDMI, resolution up to 4K @ 30Hz
LVDS/eDP, resolution up to 2560x1600 @ 60Hz

Mass Storage

eMMC 5.1 Drive soldered on-board, up to 64GB
SD 1-bit/4-bit SDIO 3.0 interface

PCI Express

Up to 1 x PCI-e x1 Gen3 port

Networking

2 x Gigabit Ethernet interface, 1x 100 Mbit Ethernet interface optional when USB Hub is equipped,
Optional WiFi 802.11a/b/g/n/ac/ax + BT 5.3 module onboard

USB

1 x USB 2.0 OTG
1x USB 3.1
USB 2.0 hub onboard, makes available
- 4 x USB 2.0 ports

Audio

1x I2S Audio interface

Serial ports

2 x UART Tx/Rx/RTS/CTS
2 x UART Tx/Rx
1 x CAN Bus

Other Interfaces

1 x 4-lanes (limited bandwidth) + 1 x 2-lanes CSI camera interfaces
I2C BUS (5x I2C Interfaces in total)
SPI interface and eSPI interfacece
13 x GPI/Os
2x PWM
Boot select signals
Power Management Signals

Power supply voltage: +5V_{DC}

RTC voltage: 3.2V

Operating temperature:

Commercial version 0°C ÷ +60°C **.
Extended version -25°C ÷ +85°C
Industrial version -40°C ÷ +85°C **.

Dimensions: 50 x82 mm (1.97" x 3.23")

Supported Operating Systems:

Linux 64-bit

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated.*

2.3 Electrical Specifications

According to SMARC specifications, the SOM-SMARC-GENIO module needs to be supplied only with an external $+5V_{DC}$ power supply.

For Real Time Clock working it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from $+5V_{DC}$ power rail.

2.3.1 Electrical characteristics

Absolute maximum ratings reflect conditions that the module may be exposed outside of the operating limits, without experiencing immediate functional failure. Functional operation is only expected during the conditions indicated under "Recommended Operating Conditions". Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the module. Exposure to absolute -maximum rated conditions for extended periods may affect device reliability.

	Pin	Min	Max	Unit
Supply Voltage	**5V_SLEEP**	-0.3	5.5	V
Supply Voltage	**VDD_RTC**	-0.3	3.5	V
Storage Temperature	$T_{Storage}$	-40	+85	°C

2.3.2 Power consumption

	Genio 510 **2GB RAM, 16GB eMMC**	**Genio 700** **4GB RAM, 32GB eMMC**
Idle	1.506W	1.643W
GPU and CPU working at full load, video reproduction of 1080p video	5.5W	5.88W
suspend	248mW	265 mW

2.3.5 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VDD_IN: Module power input voltage. +5V voltage directly coming from the card edge connector.
VDD_RTC: Low current RTC circuit backup power. 3V coin cell voltage coming from the edge card for supplying the RTC clock on the Genio 700

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +1.8V_RUN,+3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

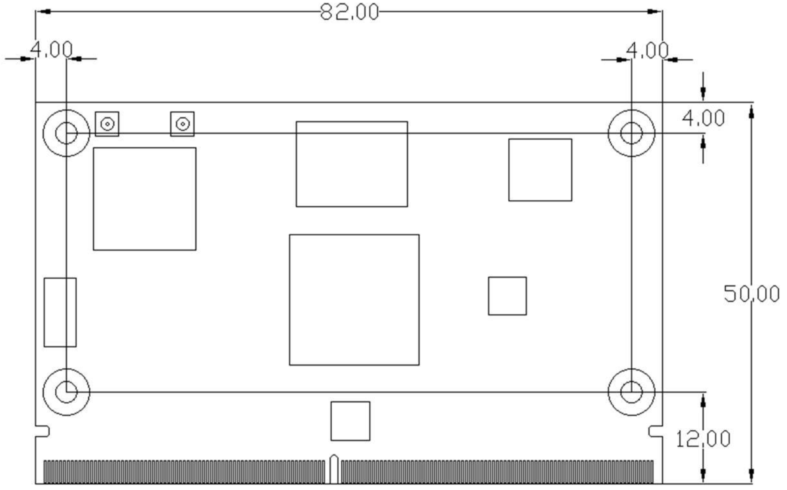
2.4 Mechanical Specifications

According to SMARC® specifications, the board dimensions are: 50 x 82 mm (1.97" x 3.23") including the pin numbering and edge finger pattern.

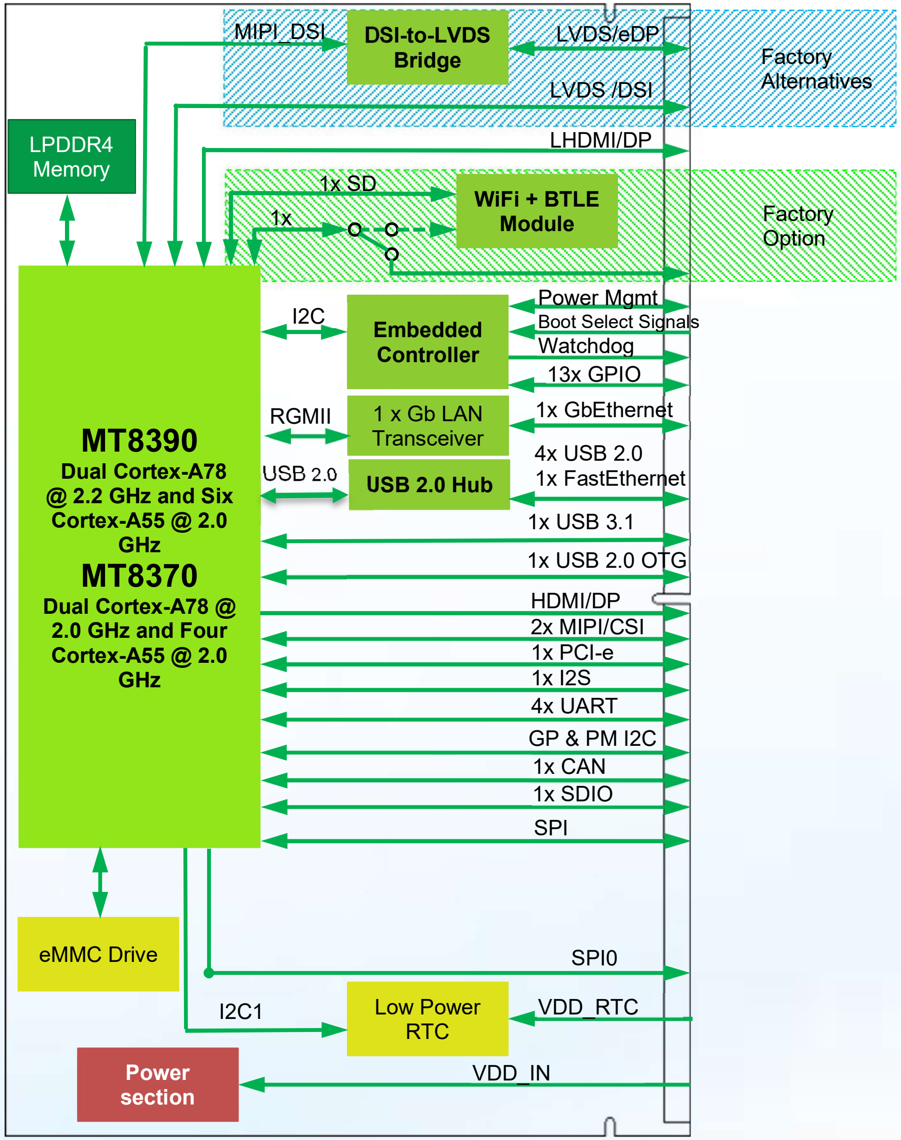
Printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs.

When using different connector heights, please consider that, according to SMARC specifications, components placed on bottom side of the module will have a maximum height of 1.3mm. Keep this value in mind when choosing the MXM connector's height, if there is the need to place components on the carrier board in the zone below the SMARC module.



2.5 Block Diagram



Chapter 3.

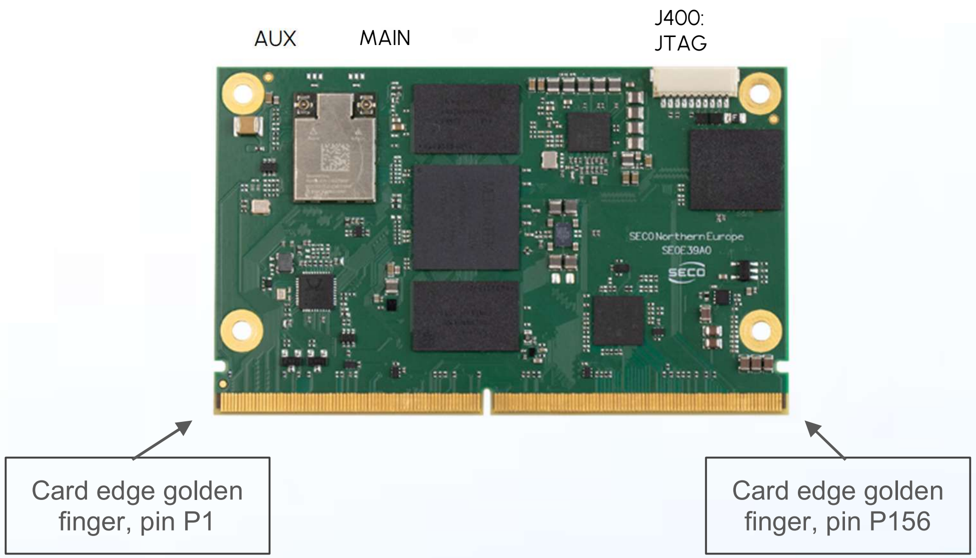
CONNECTORS

- Introduction
- Connectors description

3.1 Introduction

According to SMARC specifications, all interfaces to the board are available through a single card edge connector.

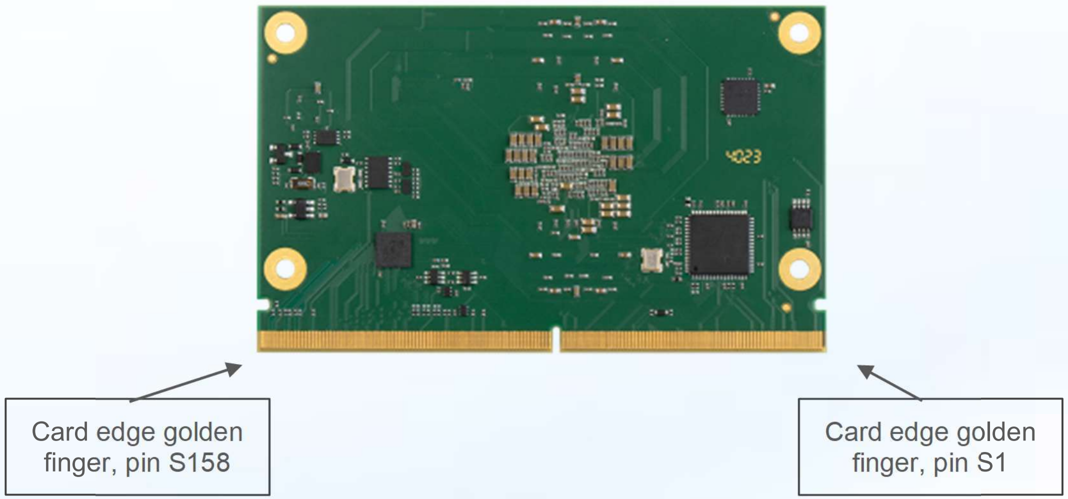
TOP SIDE



Card edge golden finger, pin P1

Card edge golden finger, pin P156

BOTTOM SIDE



Card edge golden finger, pin S158

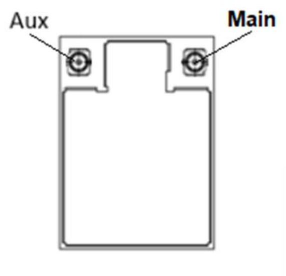
Card edge golden finger, pin S1

3.2 Connectors description

3.2.1 WiFi/BTLE Module

This SMARC® module can be equipped, by factory option, with a Dual band (2.4GHz + 5.0 GHz) WLAN 802.11 a/b/g/n/ac + BT 5.0 combo embedded module AzureWave p/n AW-CM276NF.

Aux antenna is used for WLAN and BT while main antenna is used for WLAN only. These are type IPEX MHF4 RF connectors.



3.2.2 SMARC® Connector

According to SMARC® Rel 2.1.1 specification, all interface signals are reported on the card edge connector, which is a 314-pin Card Edge that can be inserted into standard low profile 314 pin 0.5mm right pitch angle connector that was originally defined for use with MXM3 graphics cards.

Not all signals contemplated in the SMARC® Rel 2.1.1 are implemented on card edge connector, therefore, please refer to the following table for a list of effective signals reported on the card edge connector.

Consider that the signals labelled as RSVD are for factory production use only and shall be left unused, otherwise the module may not boot or function properly.

For accurate signals description, please consult the following paragraphs.

SMARC® Golden Finger Connector

TOP SIDE				BOTTOM SIDE			
SIGNAL GROUP	**Type**	**Pin name**	**Pin nr.**	**Pin nr.**	**Pin name**	**Type**	**SIGNAL GROUP**
				S1	I2C6_SCL	O	I2C
MANAGEMENT	I	SMB_ALERT_1V8#	P1	S2	I2C6_SDA	I/O	I2C
		GND	P2	S3	GND		
CAMERA	I	CSI1_CK+	P3	S4	N.C.		
CAMERA	I	CSI1_CK-	P4	S5	I2C5_SCL	O	I2C
		N.C.	P5	S6	CAM_MCK	O	CAMERA
		N.C.	P6	S7	I2C5_SDA	I/O	I2C
CAMERA	I	CSI1_RX0+	P7	S8	CSI0_CK+	I	CAMERA
CAMERA	I	CSI1_RX0-	P8	S9	CSI0_CK-	I	CAMERA
		GND	P9	S10	GND		
CAMERA	I	CSI1_RX1+	P10	S11	CSI0_RX0+	I	CAMERA
CAMERA	I	CSI1_RX1-	P11	S12	CSI0_RX0-	I	CAMERA
		GND	P12	S13	GND		
CAMERA	I	CSI1_RX2+	P13	S14	CSI0_RX1+	I	CAMERA
CAMERA	I	CSI1_RX2-	P14	S15	CSI0_RX1-	I	CAMERA
		GND	P15	S16	GND		

CAMERA	I	CSI1_RX3+	P16	S17	GBE1_MDI0+	I/O	GBE
CAMERA	I	CSI1_RX3-	P17	S18	GBE1_MDI0-	I/O	GBE
		GND	P18	S19	GBE1_LINK100#	O	GBE
GBE	I/O	GBE0_MDI3-	P19	S20	GBE1_MDI1+	I/O	GBE
GBE	I/O	GBE0_MDI3+	P20	S21	GBE1_MDI1-	I/O	GBE
GBE	O	GBE0_LINK100#	P21	S22	N.C.		
GBE	O	GBE0_LINK1000#	P22	S23	N.C.		
GBE	I/O	GBE0_MDI2-	P23	S24	N.C.		
GBE	I/O	GBE0_MDI2+	P24	S25	GND		
GBE	O	GBE0_LINK_ACT#	P25	S26	N.C.		
GBE	I/O	GBE0_MDI1-	P26	S27	N.C.		
GBE	I/O	GBE0_MDI1+	P27	S28	USB_VDD33A		
		N.C.	P28	S29	N.C.		
GBE	I/O	GBE0_MDI0-	P29	S30	N.C.		
GBE	I/O	GBE0_MDI0+	P30	S31	GBE1_LINK_ACT#	O	GBE
		N.C.	P31	S32	N.C.		
		GND	P32	S33	N.C.		
SDIO_CARD	I	SDIO_WP	P33	S34	GND		
SDIO_CARD	I/O	SDIO_CMD	P34	S35	USB4_D+	I/O	USB
SDIO_CARD	I	SDIO_CD#	P35	S36	USB4_D-	I/O	USB
SDIO_CARD	O	SDIO_CK	P36	S37	N.C.		
SDIO_CARD	O	SDIO_PWR_EN_3V3	P37	S38	I2S0_MCK	O	AUDIO
		GND	P38	S39	I2S0_LRCK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D0	P39	S40	I2S0_SDOUT	O	AUDIO
SDIO_CARD	I/O	SDIO_D1	P40	S41	I2S0_SDIN	I	AUDIO
SDIO_CARD	I/O	SDIO_D2	P41	S42	I2S0_CK	O	AUDIO
SDIO_CARD	I/O	SDIO_D3	P42	S43	N.C.		
SPI_INTERFACE	O	SPI0_CS0#	P43	S44	N.C.		
SPI_INTERFACE	O	SPI0_CK	P44	S45	N.C.		

SPI_INTERFACE	I	SPI0_DIN	P45	S46	N.C.		
SPI_INTERFACE	O	SPI0_DO	P46	S47	GND		
		GND	P47	S48	I2C_GP_CK	I/O	I2C
		N.C.	P48	S49	I2C_GP_DAT	I/O	I2C
		N.C.	P49	S50	I2S2_LRCK	I/O	AUDIO
		GND	P50	S51	I2S2_SDOUT	O	AUDIO
		N.C.	P51	S52	I2S2_SDIN	I	AUDIO
		N.C.	P52	S53	I2S2_CK	O	AUDIO
		GND	P53	S54	N.C.		
SPI_INTERFACE	O	ESPI_CS0#	P54	S55	USB5_EN_OC# (*1)	I/O	USB
		N.C.	P55	S56	ESPI_IO_2	I/O	SPI_INTERFACE
SPI_INTERFACE	O	ESPI_CK	P56	S57	ESPI_IO_3	I/O	SPI_INTERFACE
SPI_INTERFACE	I/O	ESPI_IO_1	P57	S58	N.C.		
SPI_INTERFACE	I/O	ESPI_IO_0	P58	S59	USB5_D+	I/O	USB
		GND	P59	S60	USB5_D-	I/O	USB
USB	I/O	USB0_D+	P60	S61	GND		
USB	I/O	USB0_D-	P61	S62	N.C.		
USB	I/O	USB0_EN_OC#	P62	S63	N.C.		
USB	I	USB0_VBUS_DET	P63	S64	GND		
USB	I	USB0_OTG_ID	P64	S65	N.C.		
USB	I/O	USB1_D+	P65	S66	N.C.		
USB	I/O	USB1_D-	P66	S67	GND		
USB	I/O	USB1_EN_OC#	P67	S68	USB3_D+	I/O	USB
		GND	P68	S69	USB3_D-	I/O	USB
USB	I/O	USB2_D+	P69	S70	GND		
USB	I/O	USB2_D-	P70	S71	USB2_SS_TX+	O	USB
USB	I/O	USB2_EN_OC#	P71	S72	USB2_SS_TX-	O	USB
STM32		STM32_RST#	P72	S73	GND		
		N.C	P73	S74	USB2_SS_RX+	I	USB

USB	I/O	USB3_EN_OC# (*1)	P74	S75	USB2_SS_RX-	I	USB
PCI_e	O	EXT_PCIE_A_RST# 3V3	P75	S76	N.C.		
USB	I/O	USB4_EN_OC# (*1)	P76	S77	N.C.		
PCI_e	I/O	PCIE_B_CKREQ#	P77	S78	N.C.		
PCI_e	I/O	PCIE_A_CKREQ#	P78	S79	N.C.		
		GND	P79	S80	GND		
		N.C.	P80	S81	N.C.		
		N.C.	P81	S82	N.C.		
		GND	P82	S83	GND		
PCI_e	O	PCIE_A_REFCK+	P83	S84	N.C.		
PCI_e	O	PCIE_A_REFCK-	P84	S85	N.C.		
		GND	P85	S86	GND		
PCI_e	I	PCIE_A_RX+	P86	S87	N.C.		
PCI_e	I	PCIE_A_RX-	P87	S88	N.C.		
		GND	P88	S89	GND		
PCI_e	O	PCIE_A_TX+	P89	S90	N.C.		
PCI_e	O	PCIE_A_TX-	P90	S91	N.C.		
		GND	P91	S92	GND		
SECONDARY_DISPLAY	O	HDMI_D2+	P92	S93	DP0_LANE0+	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_D2-	P93	S94	DP0_LANE0-	O	PRIMARY_DISPLAY
		GND	P94	S95	DP0_AUX_SEL	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_D1+	P95	S96	DP0_LANE1+	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_D1-	P96	S97	DP0_LANE1-	O	PRIMARY_DISPLAY
		GND	P97	S98	DP0_HPD_EXT	I	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_D0+	P98	S99	DP0_LANE2+	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_D0-	P99	S100	DP0_LANE2-	O	PRIMARY_DISPLAY
		GND	P100	S101	GND		
SECONDARY_DISPLAY	O	HDMI_CK+	P101	S102	DP0_LANE3+	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_CK-	P102	S103	DP0_LANE3-	O	PRIMARY_DISPLAY

		GND	P103	S104	N.C.		
SECONDARY_DISPLAY	I	HDMI_HPD_EXT	P104	S105	DP0_AUX+	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	I/O	HDMI_CTRL_CK	P105	S106	DP0_AUX-	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	I/O	HDMI_CTRL_DAT	P106	S107	LCD1_BKLT_EN	O	LCD_SUPPORT
		DP1_AUX_SEL	P107	S108	LVDS1_CK+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO0 / CAM0_PWR#	P108	S109	LVDS1_CK-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO1 / CAM1_PWR#	P109	S110	GND		
GPIO	I/O	GPIO2 / CAM0_RST#	P110	S111	LVDS1_0+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO3 / CAM1_RST#	P111	S112	LVDS1_0-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO4	P112	S113	EDP1_HPD_EXT		
GPIO	I/O	GPIO5	P113	S114	EDP1_HPD	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO6	P114	S115	LVDS1_1-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO7	P115	S116	LCD1_VDD_EN	O	LCD_SUPPORT
GPIO	I/O	GPIO8	P116	S117	LVDS1_2+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO9	P117	S118	LVDS1_2-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO10	P118	S119	GND		
GPIO	I/O	GPIO11	P119	S120	LVDS1_3+	O	PRIMARY_DISPLAY
		GND	P120	S121	LVDS1_3-	O	PRIMARY_DISPLAY
MANAGEMENT	I/O	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	O	LCD_SUPPORT
MANAGEMENT	I/O	I2C_PM_DAT	P122	S123	GPIO13	I/O	GPIO
BOOT_SEL	I	BOOT_SEL0#	P123	S124	GND		
BOOT_SEL	I	BOOT_SEL1#	P124	S125	LVDS0_eDP_D0+	O	PRIMARY_DISPLAY
BOOT_SEL	I	BOOT_SEL2#	P125	S126	LVDS0_eDP_D0-	O	PRIMARY_DISPLAY
MANAGEMENT	O	RESET_OUT# 1V8	P126	S127	LCD0_BKLT_EN	O	LCD_SUPPORT
MANAGEMENT	I	RESET_IN#	P127	S128	LVDS0_eDP_D1+	O	PRIMARY_DISPLAY
MANAGEMENT	I	POWER_BTN#	P128	S129	LVDS0_eDP_D1-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_TX	P129	S130	GND		
ASYNC_SERIAL	I	SER0_RX	P130	S131	LVDS0_TX2+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_RTS#	P131	S132	LVDS0_TX2-	O	PRIMARY_DISPLAY

ASYNC_SERIAL	I	SER0_CTS#	P132	S133	LCD0_VDD_EN	O	LCD_SUPPORT
		GND	P133	S134	LVDS0_eDP_CK+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER1_TX	P134	S135	LVDS0_eDP_CK-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER1_RX	P135	S136	GND		
ASYNC_SERIAL	O	SER2_TX	P136	S137	LVDS0_TX3+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER2_RX	P137	S138	LVDS0_TX3-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER2_RTS#	P138	S139	I2C0_SCL	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER2_CTS#	P139	S140	I2C0_SDA	I/O	LCD_SUPPORT
ASYNC_SERIAL	O	SER3_TX	P140	S141	LCD0_BKLT_PWM	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER3_RX	P141	S142	GPIO12	I/O	GPIO
		GND	P142	S143	GND		
CAN	O	CAN0_TX	P143	S144	eDP0_HPD_EXT	I	PRIMARY_DISPLAY
CAN	I	CAN0_RX	P144	S145	WDT_TIME_OUT#	O	WATCHDOG
		N.C.	P145	S146	PCIE_WAKE#	I	PCI_e
		N.C.	P146	S147	VDD_RTC		
		VDD_IN	P147	S148	LID#	I	MANAGEMENT
		VDD_IN	P148	S149	SLEEP#	I	MANAGEMENT
		VDD_IN	P149	S150	VIN_PWR_BAD#	I	MANAGEMENT
		VDD_IN	P150	S151	CHARGING#	I	MANAGEMENT
		VDD_IN	P151	S152	CHARGER_PRSNT#	I	MANAGEMENT
		VDD_IN	P152	S153	CARRIER_STBY# 1V8	O	MANAGEMENT
		VDD_IN	P153	S154	CARRIER_PWR_ON 1V8	O	MANAGEMENT
		VDD_IN	P154	S155	FORCE_RECOV#	I	BOOT_SEL
		VDD_IN	P155	S156	BATLOW#	I	MANAGEMENT
		VDD_IN	P156	S157	TEST#	I	MANAGEMENT
				S158	GND		

(*1) Connected to GND when no Hub

!

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3.2.2.1 LCD Display Support Signals

The panel control signals are:

LCD1_VDD_EN: Panel #1 VDD enable signal. Set high to enable. +1.8V_RUN electrical level Output

LCD1_BKLT_EN: Panel #1 Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_RUN electrical level Output.

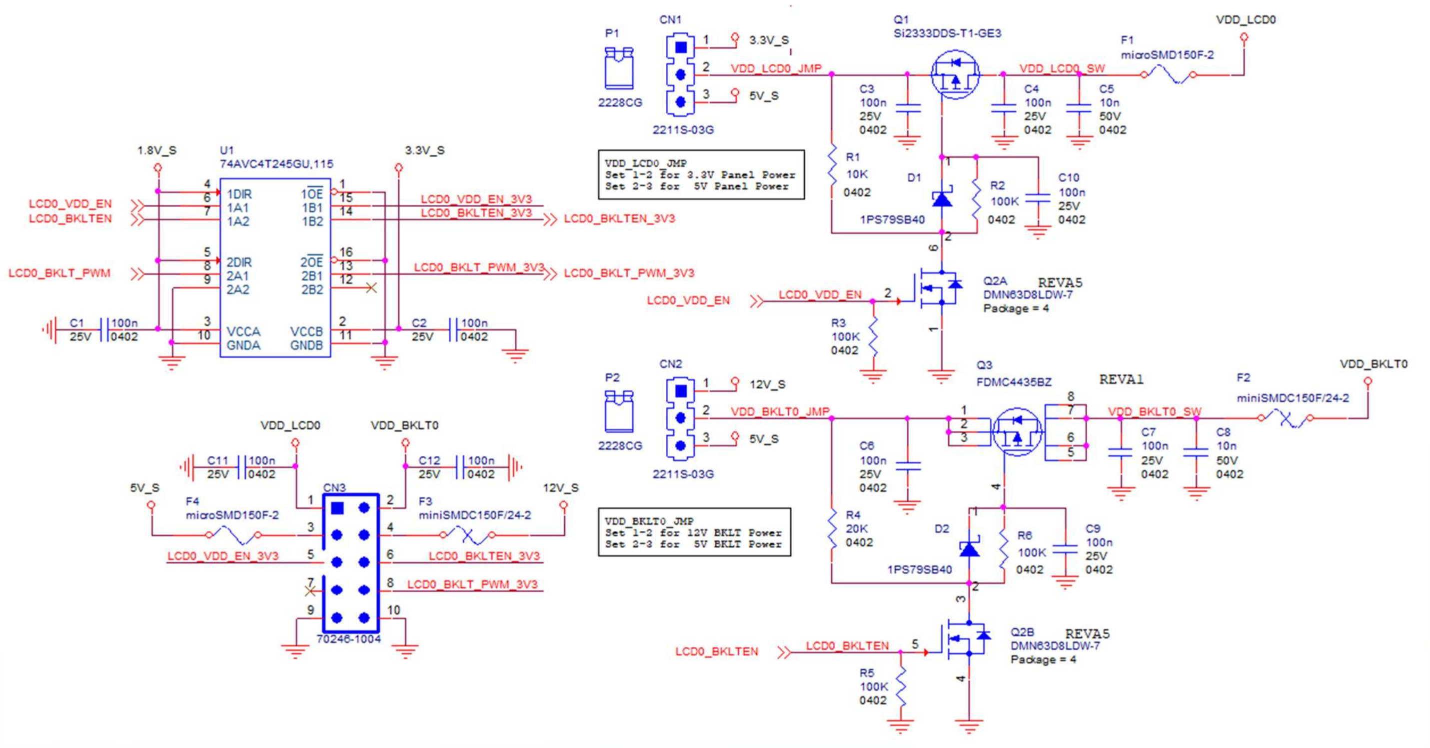
LCD1_BKLT_PWM: This signal can be used to adjust the Panel #1 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_RUN electrical level Output.

I2C LCD signals are managed by SoC I2C0 bus.

I2C_LCD_DAT: LCD I2C Data. This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level Bidirectional with a 2k2Ω pull-up resistor.

I2C_LCD_CLK: LCD I2C Clock: This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level Output with a 2k2Ω pull-up resistor.

Please refer to the following schematics as an example of connection of LCD display control signals and supply voltage selection jumpers.



3.2.2.2 eDP / Dual Channel LVDS (factory alternatives)

A dual channel LVDS interface is natively supported by the SOC, with a maximum supported resolution of 1920x1200 @ 60Hz, while an eDP interface can be selected as a factory alternative to be present on the edge pinout in place of Channel #0 of the LVDS interface.

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for Channel #0 are LVDS:

LVDS0_0+/LVDS0_0-: LVDS Channel #0 differential data pair #0.

LVDS0_1+/LVDS0_1-: LVDS Channel #0 differential data pair #1.

LVDS0_2+/LVDS0_2-: LVDS Channel #0 differential data pair #2.

LVDS0_3+/LVDS0_3-: LVDS Channel #0 differential data pair #3.

LVDS0_CK+/LVDS0_CK-: LVDS Channel #0 differential Clock.

OR the signals for Channel #0 are eDP:

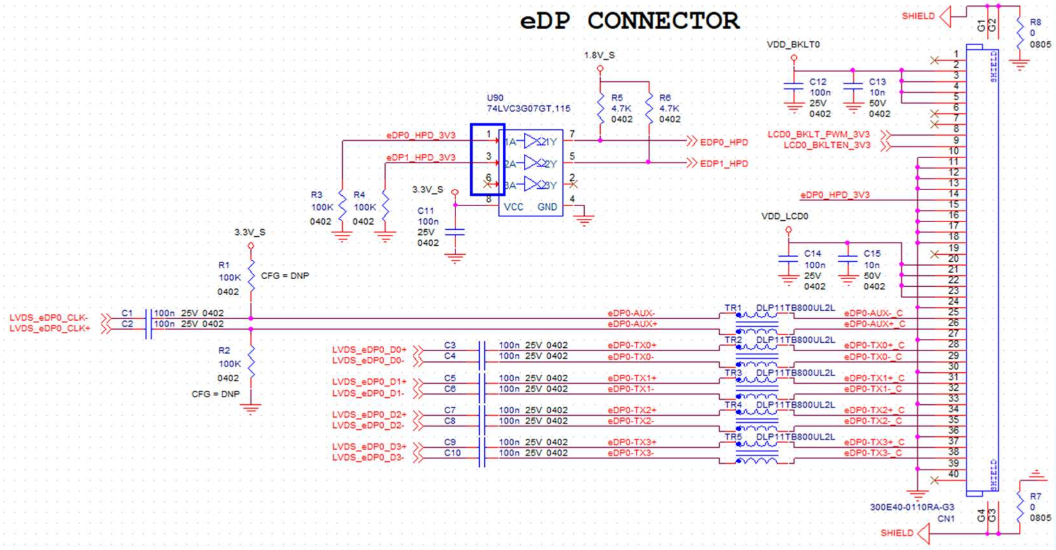
eDP0_D0+/ eDP0_D0-: eDP Channel #0 differential data pair #0.

eDP0_D1+/ eDP0_D1-: eDP Channel #0 differential data pair #1.

eDP0_AUX+/ eDP0_AUX-: eDP Channel #0 differential Clock.

eDP0_HPD: Hot Plug Detect, Active high Input signal of +1.8V_RUN electrical level from carrier board. 1MΩ pull-down resistor is placed on module for this signal.

Please refer to the following schematics as an example of connection of eDP interface on the carrier board. Hot Plug Detect signal must be buffered to prevent back feeding of power from the display to the module as well as level translation.



The signals for Channel #1 of the LVDS interface is always available on the edge pinout regardless of the factory board configuration.

LVDS1_1+ / LVDS1_0- : LVDS Channel #1 differential data pair #0

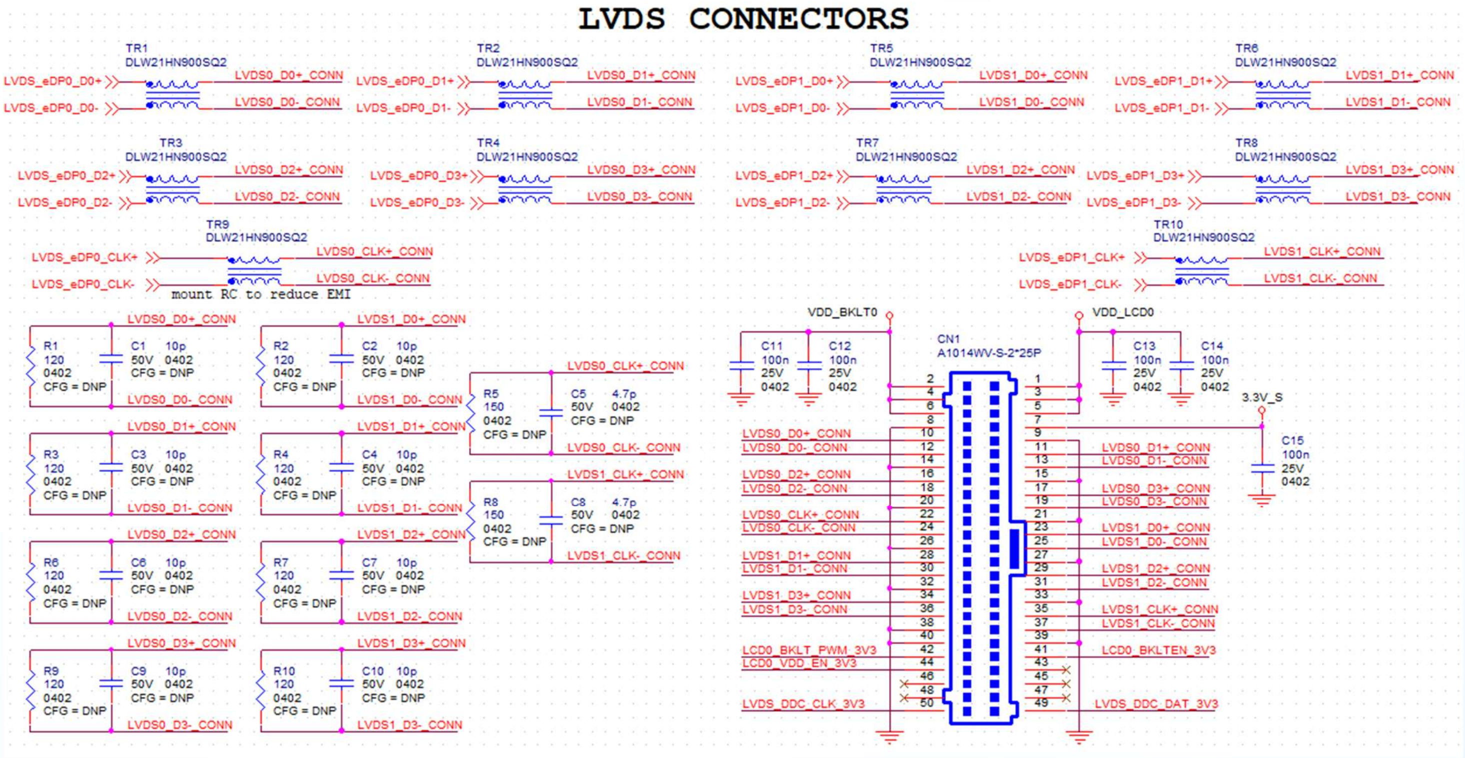
LVDS1_1+/ LVDS1_1-: LVDS Channel #1 differential data pair #1

LVDS1_2+/LVDS1_2-: LVDS Channel #1 differential data pair #2

LVDS1_3+/ LVDS1_3-: LVDS Channel #1 differential data pair #3

LVDS1_CK+/ LVDS1_CK-: LVDS Channel #1 differential Clock

Please refer to the following schematics as an example of connection of dual channel LVDS interface on the carrier board, with EMI filtering section included.



3.2.2.3 Secondary Display (HDMI interface) signals

The MediaTek GENIO 510 / 700 processor has an HD Display Transmitter Controller (HDMI TX), which provides a HDMI interface with resolution limited by the NXP SoC up to 3840x2160 @ 30Hz.

The signals are:

HDMI_D0+/HDMI_D0-: HDMI Output Differential Pair #0

HDMI_D1+/HDMI_D1-: HDMI Output Differential Pair #1

HDMI_D2+/HDMI_D2-: HDMI Output Differential Pair #2

HDMI_CK+/HDMI_CK-: HDMI Differential Clock

HDMI_HPD: Hot Plug Detect Input signal. +1.8V_RUN electrical level signal

HDMI_CTRL_CK: DDC Clock line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

Since HDMI Tx module is embedded in the i.MX 8M processors it is not necessary to implement voltage level shifter for TMDS differential pairs on the Carrier board. It is still necessary, however, to implement voltage level shifters on Control data/Clock signals, as well as for Hot Plug Detect signal.

3.2.2.4 Serial Cameras

There are two MIPI-CSI interfaces available. The CSI0 interface supports two lanes, the CSI1 interface supports 4 lanes with limited bandwidth. Consider that from the SoC the CSI0 interface is managed by the MIPI_CSI0 group signals and I2C5 bus, while CSI1 is managed by MIPI_CSI1 group signals and I2C6 bus.

CSI0_CK+/CSI0_CK-: 2-lane CSI Input Clock Differential Pair
CSI0_RX0+/CSI0_RX0-: 2-lane CSI Input Differential Pair 0
CSI0_RX1+/CSI0_RX1-: 2-lane CSI Input Differential Pair 1

CSI1_CK+/CSI1_CK-: 4-lane CSI Input Clock Differential Pair
CSI1_RX0+/CSI1_RX0- 4-lane CSI Input Differential Pair 0
CSI1_RX1+/CSI1_RX1-: 4-lane CSI Input Differential Pair 1
CSI1_RX2+/CSI1_RX2-: 4-lane CSI Input Differential Pair 2
CSI1_RX3+/CSI1_RX3-: 4-lane CSI Input Differential Pair 3

CAM_MCK: Master clock Output for CSI Port #0 and/or #1 support, electrical level 1.8V_RUN

I2C_CAM0_CK: CSI Port #0 dedicated I2C5 Bus Clock signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.
I2C_CAM0_DAT: CSI Port #0 dedicated I2C5 Bus Data signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

3.2.2.5 SDI/O interface signals

The MediaTek GENIO 510 / 700 processors offer many different SDIO interfaces, that can be used independently one from the other to implement different mass storages (internal eMMC, internal SD Card, external SDI/O interface).

The MSDC0 signals of the processor are used for the onboard eMMC storage of the module.

The MSDC2 signals of the processor are used for the factory optional onboard WiFi/BTLE module.

The MSDC1 interface of the processor is externally accessible through the edge connector of the module. Supporting 4-bit mode as per the SMARC specification.

The uSDHC controller complies with:

- SD Host Controller Standard Specification version 3.0 with SDR104 signaling to support up to 104MB/sec.
- MMC System Specification version 5.0

The edge accessible MSDC1 signals are as follows:

SDIO_WP: Write Protect bidirectional signal, electrical level +1.8V_RUN (SDR104) or +3.3V_RUN with 10kΩ pull-up resistor. It is used to communicate the status of Write Protect switch on external SD/MMC card.

SDIO_CMD: Command/Response line. Used to send command from Host (MicroTek Genio 510/ 700) to the connected card, and to send the response from the card to the Host.

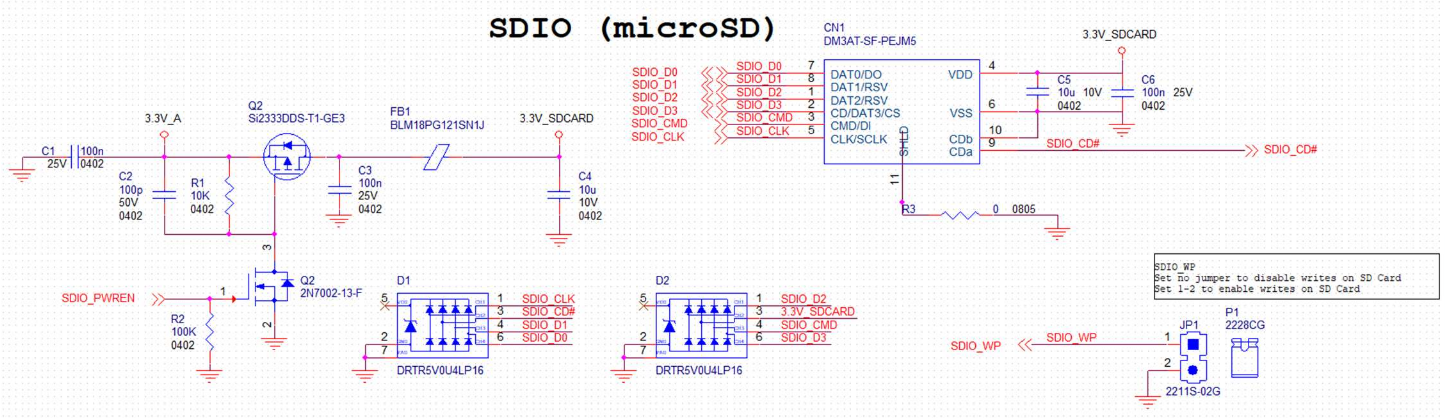
SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +1.8V_RUN (SDR104) or +3.3V_RUN with 10kΩ pull-up resistor. This signal must be externally pulled low to signal that a SDIO/MMC Card is present.

SDIO_CK: Clock Line (output), up to 200MHz maximum frequency for SDR104 Mode (4-bit only).

SDIO_PWR_EN: SDIO Power Enable output, active high signal, electrical level +1.8V_RUN (SDR104) or +3.3V_RUN with 2.2kΩ pull-up resistor. It is used to enable the power line supplying SD/SDIO/MMC devices.

SDIO_[D0÷D3]: SDIO data bus. Signals for 4-bit SD/SDIO/MMC communication mode.

Please refer to the following schematics as an example of connection of SDIO interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression.



3.2.2.6 SPI interface signals

The signals related to SPI0 are as follows:

SPI0_CS0#: SPI primary Chip select, active low output signal. Electrical level +1.8V_RUN

SPI0_CS1#: SPI secondary Chip select, active low output signal. Electrical level +1.8V_RUN. This signal must be used only in case there are two SPI devices on the carrier board, and the first chip select signal (SPI_CS0#) has already been used. It must not be used in case there is only one SPI device

SPI0_CK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +1.8V_RUN

SPI0_DIN: SPI0 Master Data Input, electrical level +1.8V_RUN. Input to GENIO 510 / 700 from SPI devices embedded on the Carrier Board.

SPI0_DO: SPI0 Master Data Output, electrical level +1.8V_RUN. Output from GENIO 510 / 700 to SPI devices embedded on the Carrier Board

The signals related to ESPI are as follows:

ESPI_CS0#: SPI primary Chip select, active low output signal. Electrical level +1.8V_RUN.

ESPI_CK: SPI Master Clock Output. Electrical level +1.8V_RUN. The reference timing signal for all the serial input and output operations

ESPI_IO_[0:3]: SPI Master Data Bidirectional . Electrical level +1.8V_RUN. Data transfer between the master and slaves. In Single I/O mode, ESPI_IO_0 is the ESPI master output/ESPI slave input (MOSI) whereas ESPI_IO_1 is the ESPI master input/QSPI slave output (MISO).

SPI interface can support speed up to 20MHz.

3.2.2.7 Audio interface signals

Here are following the signals related to I2S Audio interfaces:

AUDIO_MCK: Master clock output to Audio codec. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_LRCK: Left& Right audio synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDOUT: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDIN: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2S2_LRCK: Left& Right audio synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2S2_SDOUT: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S2_SDIN: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN

I2S2_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

Signals routed to the Carrier Board have to be connected to I2S Audio Codecs. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.2.8 I2C Interface

I2C General Purpose signals are managed by SoC I2C4 bus.

I2C_GP_CK: I2C General Purpose clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor

I2C_GP_DAT: I2C General Purpose data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor

I2C Power Management signals are managed by SoC I2C3 bus.

I2C_PM_CK: Power management clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_ALW with 2.2kΩ pull-up resistor.

I2C_PM_DAT: Power management data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_ALW with 2.2kΩ pull-up resistor

On this bus a selection of addresses must be left reserved for on-board peripherals as presented in this table:

I2C3 Bus

Address	**Peripheral**
0x40	Embedded Controller

3.2.2.9 Asynchronous Serial Ports (UART) interface signals

All UART interface signals are directly managed by the GENIO 510 / 700. In all versions, the edge connector offers the four following UART interfaces.

SER0_TX: UART #2 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

SER0_RX: UART #2 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER0_RTS#: UART #2 Interface, Handshake signal, Request to Send (output) line, +1.8V_RUN electrical level

SER0_CTS#: UART #2 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER1_TX: UART #4 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

SER1_RX: UART #4 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER2_TX: UART #3 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

SER2_RX: UART #3 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER2_RTS#: UART #3 Interface, Handshake signal, Request to Send (output) line, +1.8V_RUN electrical level

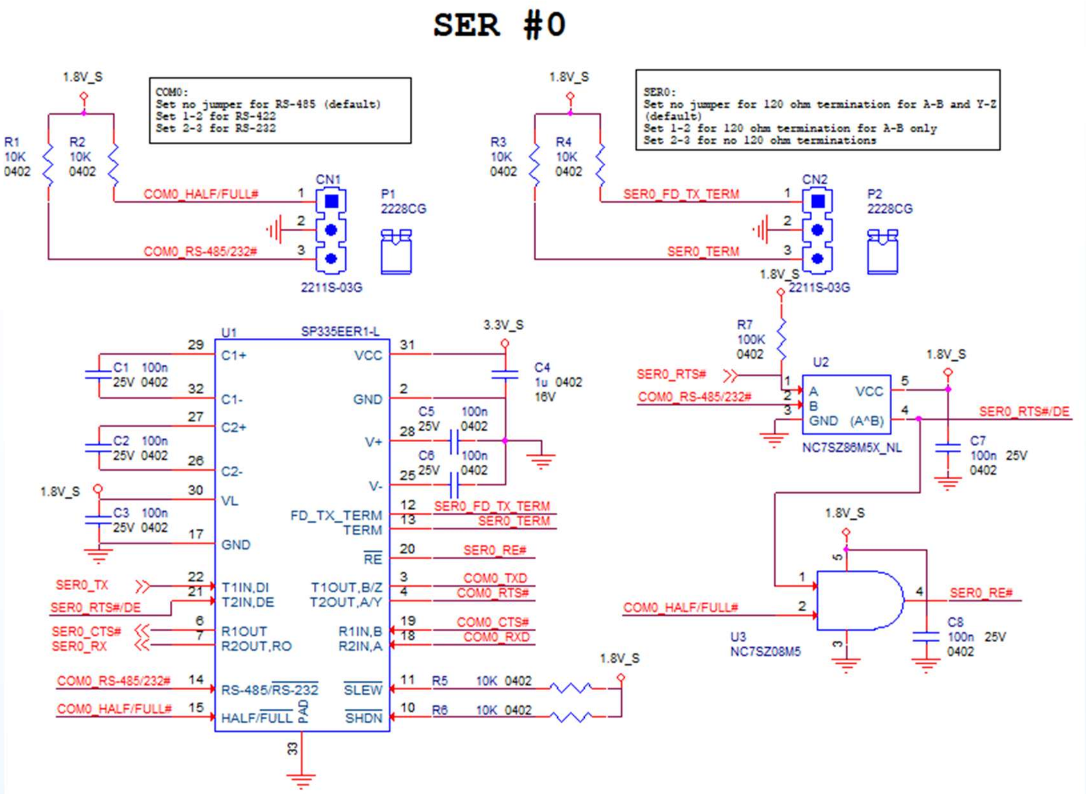
SER2_CTS#: UART #3 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor.

SER3_RX: UART #1 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER3_TX: UART #1 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

Please consider that interface is at +1.8V_RUN electrical level; therefore, please evaluate well the typical scenario of application. If there isn't any explicit need of interfacing directly at +1.8V_RUN level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

In the following schematic here is an example of UART interface on the carrier board, with a multiprotocol transceiver allowing to support RS485/RS-422/RS-232 serial interfaces.



COM0:
Set no jumper for RS-485 (default)
Set 1-2 for RS-422
Set 2-3 for RS-232

SER0:
Set no jumper for 120 ohm termination for A-B and Y-Z (default)
Set 1-2 for 120 ohm termination for A-B only
Set 2-3 for no 120 ohm terminations

3.2.2.10 USB interface signals

The module has up to 5x USB ports (With Hub -> 5 Ports , without Hub -> 2 Ports)consisting of 1x USB 2.0 port from the MediaTek GENIO 510 / 700 processor USB 2.0 controller which can be configured at kernel compile time to work as Host or Client (USB0). One Superspeed USB-Port (USB2), 4x USB 2.0 from a Cypress USB3304-68LTXC USB 3.0 hub controller(USB-Port 1,3,4,5).

Here following the signals related to USB interfaces.

USB0+/ USB0-: Universal Serial Bus 2.0 Port #0 differential pair (directly managed by GENIO 510 / 700 USB Host Controller core #1).

USB0_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for over current operation information.
The USB0 port is directly managed by Genio 700 USB Host Controller core #1 and can be used for serial download driving FORCE_RECOV# low.
Please take note that the OTG functionality on this port is not supported at runtime, USB0 must be set to work as Client or Host at kernel compile time.

USB1+/ USB1-: Universal Serial Bus Port 2.0 #1 differential pair.

USB1_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for OC operation information.

USB2+/USB2-: Universal Serial Bus Port 2.0 #2 differential pair.

USB2_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for OC operation information.

USB2_SSTX+/ USB2_SSTX-: USB 3.0 Port #1 Superspeed Transmit differential pair.

USB2_SSRX+/ USB2_SSRX-: USB 3.0 Port #1 Superspeed Receive differential pair.

USB3+/USB3-: Universal Serial Bus Port 2.0 #3 differential pair.

USB3_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for OC operation information.

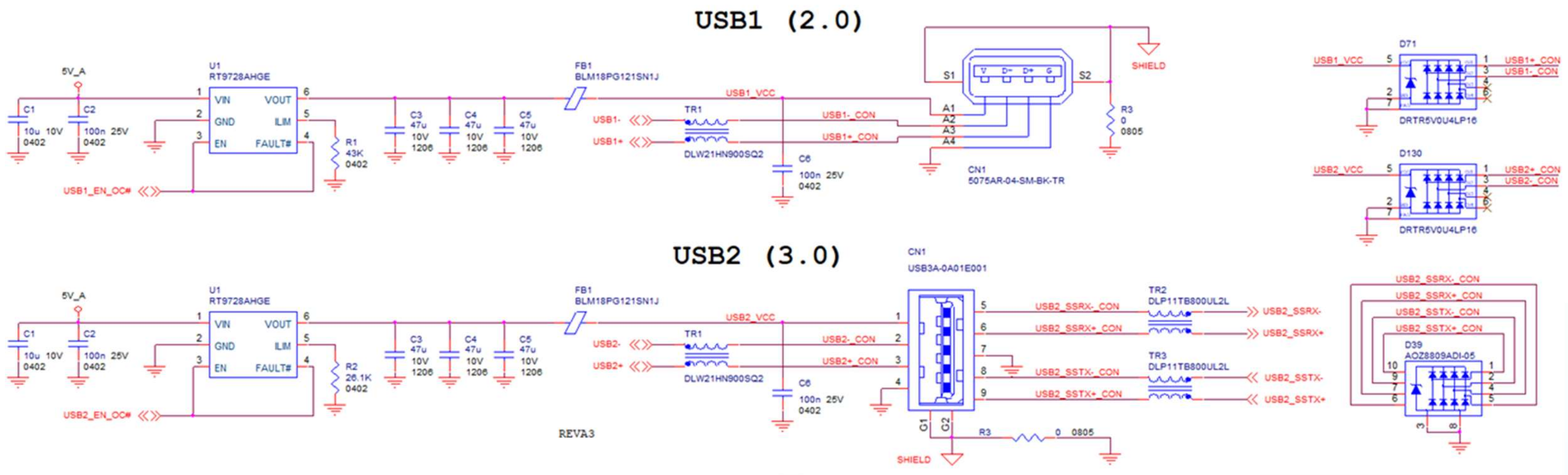
USB4+/USB4-: Universal Serial Bus Port 2.0 #4 differential pair.

USB4_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for OC operation information.

USB5+/USB5-: Universal Serial Bus Port 2.0 #5 differential pair.

USB5_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for OC operation information.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed. Switch with settable current limit on power lines are recommended.



3.2.2.11 PCI Express interface signals

The module can offer one PCI Express x1 lanes, which is directly managed by MediaTek Genio 510 / 700 processor (PCI express Gen 3.0 is supported).

Here following the signals involved in PCI express management

PCIE_A_RX+/ PCIE_A_RX-: PCI Express lane #0, Transmitting Output Differential pair
PCIE_A_TX+/PCIE_A_TX-: PCI Express lane #0, Receiving Input Differential pair
PCIE_A_REFCK+/ PCIE_A_REFCK-: PCI Express Reference Clock for lane #0, Differential Pair
PCIE_A_RST#: Reset Signal that is sent from SMARC® Module to a PCI-e device available on the carrier board. Active Low, +3.3V_RUN electrical level.
PCIE_A_CKREQ#: PCIe Port A clock request, can be used for power saving mode on PCIe. Active low, driven by open drain circuitry on the carrier board.
PCIE_WAKE#: PCIe wake up interrupt to host input signal. Active low, +3.3V_ALW electrical level.

3.2.2.12 Gigabit Ethernet signals

The Gigabit Ethernet interface is realized on the module by using the Realtek RTL8211FI Gigabit Ethernet transceivers, which are interfaced to MediaTek Genio 510 / 700 processor through RGMII interface.

Here following the signals involved in Gigabit Ethernet #0 management:

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) Transmit differential pair

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) Transmit differential pair

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) Transmit differential pair

GBE0_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE0_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

Here following the signals involved in Fast Ethernet #1 management:

GBE1_MDI0+/GBE1_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair

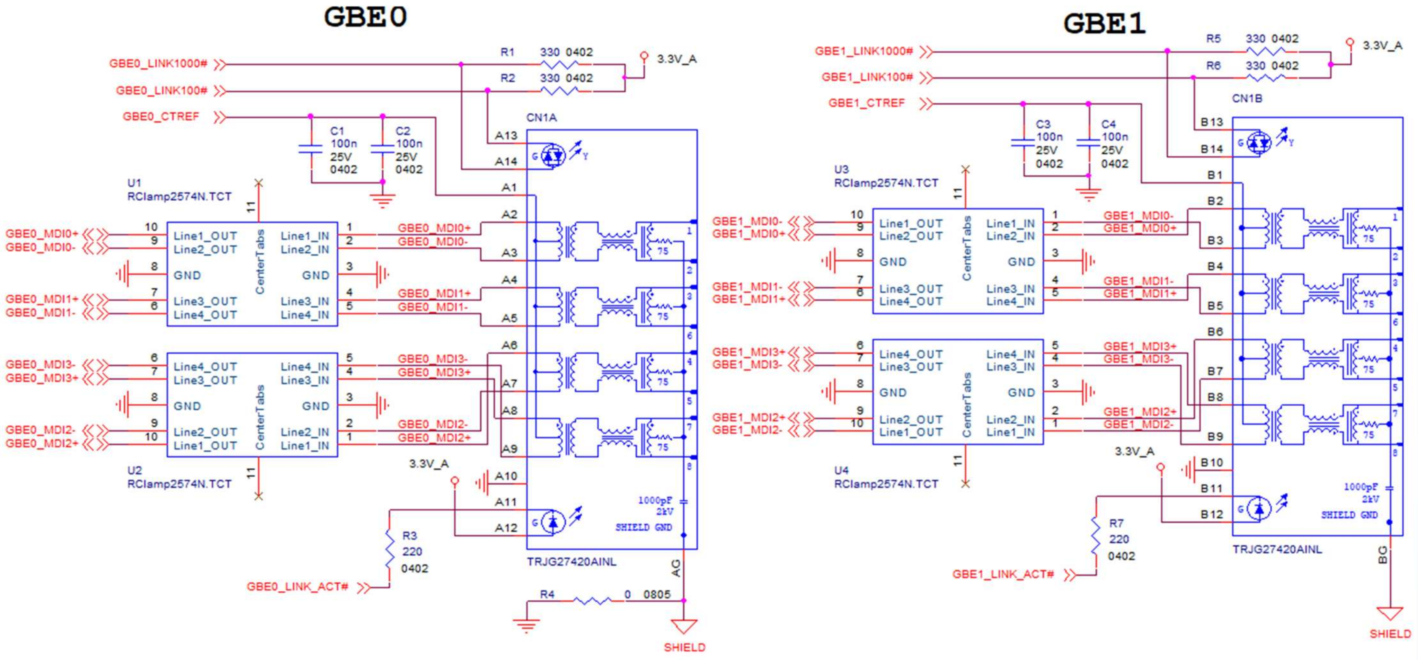
GBE1_MDI1+/GBE1_MDI1-: Media Dependent Interface (MDI) Transmit differential pair

GBE1_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE1_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

Please refer to the following schematics as an example of connection of Ethernet interface on the carrier board, with TVS diodes specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. For the REALTEK Gigabit Ethernet PHY transceiver, however, doesn't need the analog powered centre tap, therefore the signal GBE0_CTREF is not available on SMARC® connector.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary, for the Gigabit Etherner interfaces. The second Ethernet Port is by default FastEthernet.



3.2.2.13 CAN interface signals

The CAN interface signals are managed by a MCP2518 SPI to CAN converter.

CAN0_TX: CAN Transmit Output for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal with a 2k2Ω pull-up resistor

CAN0_RX: CAN Receive Input for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal with a 2k2Ω pull-up resistor

Please consider that it is not possible to connect the SMARC® CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

3.2.2.14 Watchdog

WDT_TIME_OUT#: Watchdog timer Output. +1.8V_RUN electrical level

3.2.2.15 Miscellaneous signals

GPIO0 / CAM0_PWR#: General Purpose I/O #0, +1.8V_RUN electrical level
GPIO1 / CAM1_PWR#: General Purpose I/O #1, +1.8V_RUN electrical level
GPIO2 / CAM0_RST#: General Purpose I/O #2, +1.8V_RUN electrical level
GPIO3 / CAM1_RST#: General Purpose I/O #3, +1.8V_RUN electrical level
GPIO4: General Purpose I/O #4, +1.8V_RUN electrical level
GPIO5: General Purpose I/O #5, +1.8V_RUN electrical level
GPIO6: General Purpose I/O #6, +1.8V_RUN electrical level
GPIO7: General Purpose I/O #7, +1.8V_RUN electrical level
GPIO8: General Purpose I/O #8, +1.8V_RUN electrical level
GPIO9: General Purpose I/O #9, +1.8V_RUN electrical level
GPIO10: General Purpose I/O #10, +1.8V_RUN electrical level
GPIO11: General Purpose I/O #11, +1.8V_RUN electrical level
GPIO12: General Purpose I/O #12, +1.8V_RUN electrical level
GPIO13: General Purpose I/O #11, +1.8V_RUN electrical level

3.2.2.16 Management pins

According to the SMARC® specifications, the input pins listed below are all Active Low, meant to be driven by open drain devices on the carrier board:

VIN_PWR_BAD#: Power Bad indication signal from the Carrier Board
CARRIER_PWR_ON: Power On. Command to the Carrier Board. Output, +1.8V_ALW electrical level
CARRIER_STBY#: Stand By command to the Carrier Board. Output, +1.8V_ALW electrical level
RESET_OUT#: General Purpose Reset. Output, +1.8V_ALW electrical level
RESET_IN#: General Purpose Reset. Input, +3.3V_ALW electrical level
POWER_BTN#: Power Button. Input, +3.3V_ALW electrical level
SLEEP#: Sleep indicator from Carrier board. Input, +3.3V_ALW electrical level (Standby not supported)
LID#: LID Switch. Input, +3.3V_ALW electrical level
BATLOW#: Battery Low indication signal from the Carrier Board. Input, +3.3V_ALW electrical level
CHARGING#: Battery Charging Input Signal from the Carrier Board. Input, +3.3V_ALW electrical level

CHARGER_PRSNT#: Battery Charger Present input from the Carrier Board. Input, +3.3V_ALW electrical level
TEST#: Held low by Carrier to invoke Module vendor specific test function(s). Input. +3.3V_ALW electrical level with a 10kΩ pull-up resistor
SMB_ALERT_1V8#: SM Bus Alert# (interrupt) signal. Input, +1.8V_ALW electrical level with a 2k2Ω pull-up resistor

3.2.2.17 Boot Select

The following signals are active low and driven by open drain circuitry on the carrier board.

BOOT_SEL0#: Boot Device Selection #0. Input, +3.3V_ALW electrical level with a 10kΩ pull-up resistor
BOOT_SEL1#: Boot Device Selection #1. Input, +3.3V_ ALW electrical level with a 10kΩ pull-up resistor
BOOT_SEL2#: Boot Device Selection #2. Input, +3.3V_ ALW electrical level with a 10kΩ pull-up resistor
FORCE_RECOV#: Force recovery Mode. Input, +3.3V_ ALW electrical level with a 10kΩ pull-up resistor

Chapter 4.

Appendices

- SoC to Connector Pinout
- Thermal Design
- What's different in Rev.A / Rev.B ?

4.1 SoC to Connector Pinout

Some of the signals available on the SMARC® Edge Connector can be reprogrammed to implement different functionalities, according to the Genio pin-multiplexing possibilities.
In this table is presented the list of connector signals which are connected to the SoC with the corresponding SoC pad and name. Consult the Genio documentation for the multiplexing capabilities of the listed pads.

SMARC® Golden Finger Connector

TOP SIDE				**BOTTOM SIDE**			
SoC signal	**SoC pad**	**Pin name**	**Pin nr.**	**Pin nr.**	**Pin name**	**SoC pad**	**SoC signal**
				S1	I2C6_SCL	H7	SCL6
			P1	S2	I2C6_SDA	G6	SDA6
			P2	S3			
CSI1A_L2P_T1B	K7	CSI1_CK+	P3	S4			
CSI1A_L2P_T1C	K6	CSI1_CK-	P4	S5	I2C5_SCL	F5	SCL5
			P5	S6	CAM_MCK	E4	CMMCLK0
			P6	S7	I2C5_SDA	F6	SDA5
CSI1A_L1P_T0C	J2	CSI1_RX0+	P7	S8	CSI0_CK_P	M6	CSI0A_L2P_T1B
CSI1A_L1N_T1B	J3	CSI1_RX0-	P8	S9	CSI0_CK_N	N6	CSI0A_L2N_T1C
			P9	S10			
CSI1B_L0P_T0A	K5	CSI1_RX1+	P10	S11	CSI0_RX0_P	N4	CSI0A_L1P_T0C
CSI1B_L0N_T0B	K3	CSI1_RX1-	P11	S12	CSI0_RX0_N	N5	CSI0A_L1N_T1A
			P12	S13			
CSI1A_L0P_T0A	J5	CSI1_RX2+	P13	S14	CSI0_RX1_P	P2	CSI0B_L0N_T0B
CSI1A_L0N_T0B	J4	CSI1_RX2-	P14	S15	CSI0_RX1-N	P1	CSI0B_L0N_T0B
			P15	S16			
CSI1B_L1P_T0C	L3	CSI1_RX3+	P16	S17			

CSI1B_L1N_T1A	L4	CSI1_RX3-	P17	S18			
			P18	S19			
			P19	S20			
			P20	S21			
			P21	S22			
			P22	S23			
			P23	S24			
			P24	S25			
			P25	S26			
			P26	S27			
			P27	S28			
			P28	S29			
			P29	S30			
			P30	S31			
			P31	S32			
			P32	S33			
			P33	S34			
MSDC1_CMD	D3	SDIO_CMD	P34	S35			
GPIO02	Y6	SDIO_CD#	P35	S36			
MSDC1_CLK	D4	SDIO_CK	P36	S37			
GPIO04	Y8	SDIO_PWR_EN	P37	S38	I2SO2_MCK	H34	I2SO2_MCK
			P38	S39	I2S0_LRCK	J34	I2SO2_WS
MSDC1_DATA0	D2	SDIO_D0	P39	S40	I2S0_SDOUT	J33	I2SO2_D0
MSDC1_DATA1	D1	SDIO_D1	P40	S41	I2S0_SDIN	J37	I2SIN_D0
MSDC1_DATA2	C4	SDIO_D2	P41	S42	I2S0_CK	H33	I2S02_BCK
MSDC1_DATA3	C3	SDIO_D3	P42	S43			
SPIM1_CSB	T9	SPI0_CS0#	P43	S44			
SPIM1_CLK	T10	SPI0_CK	P44	S45			
SPIM1_MISO	T7	SPI0_DIN	P45	S46			

SPIM1_MOSI	T8	SPI0_DO	P46	S47			
			P47	S48	I2C_GP_CK	K36	SCL4
			P48	S49	I2C_GP_DAT	K37	SDA4
			P49	S50	I2S2_LRCK	J36	I2SIN_WS
			P50	S51	I2S2_SDOUT	G31	I2S02_D1
			P51	S52	I2S2_SDIN	G33	I2SIN_D1
			P52	S53	I2S2_CK	H36	I2SIN_BCK
			P53	S54			
DMIC1_DAT	N31	ESPI_CS0#	P54	S55			
			P55	S56	ESPI_IO_2	P33	DMIC2_DAT
DMIC1_CLK	N30	ESPI_CK	P56	S57	ESPI_IO_3	P35	DMIC2_DAT_R
DMIC2_CLK	N34	ESPI_IO_1	P57	S58			
DMIC1_DAT_R	P30	ESPI_IO_0	P58	S59			
			P59	S60			
USB_DP_P0	W32	USB0+	P60	S61			
USB_DM_P0	W31	USB0-	P61	S62			
			P62	S63			
			P63	S64			
USB0_ID_DIG	R36	USB0_OTG_ID	P64	S65			
			P65	S66			
			P66	S67			
			P67	S68			
			P68	S69			
USB_DP_P1	U37	USB2+	P69	S70			
USB_DM_P1	U36	USB2-	P70	S71	USB2_SS_TX+	Y33	SSUSB_TXP
			P71	S72	USB2_SS_TX-	Y34	SSUSB_TXN
			P72	S73			
			P73	S74	USB2_SS_RX+	W37	SSUSB_RXP
			P74	S75	USB2_SS_RX-	W36	SSUSB_RXN

PCIE_PERESET_N	AA3	PCIE_A_RST#	P75	S76			
			P76	S77			
PCIE_CLKREQ_N	AA1	PCIE_B_CKREQ#	P77	S78			
			P78	S79			
			P79	S80			
			P80	S81			
			P81	S82			
			P82	S83			
PCIE_CKP	AN4	REF_CLKP_CARRIER	P83	S84			
PCIE_CKN	AN3	REF_CLKN_CARRIER	P84	S85			
			P85	S86			
PCIE_LN0_RXP	AP2	PCIE_RXP_CARRIER	P86	S87			
PCIE_LN0_RXN	AP1	PCIE_RXN_CARRIER	P87	S88			
			P88	S89			
PCIE_ LN0_TXP	AM1	PCIE_TXP_CARRIER	P89	S90			
PCIE_ LN0_TXN	AM2	PCIE_TXN_CARRIER	P90	S91			
			P91	S92			
HDMITX21_CH2_P	AK35	HDMI_D2+	P92	S93	DP0_LANE0+	AG35	DP_LN0_TXP
HDMITX21_CH2_M	AL35	HDMI_D2-	P93	S94	DP0_LANE0-	AH35	DP_LN0_TXN
			P94	S95			
HDMITX21_CH1_P	AM36	HDMI_D1+	P95	S96	DP0_LANE1+	AH32	DP_LN1_TXP
HDMITX21_CH1_M	AM37	HDMI_D1-	P96	S97	DP0_LANE1-	AH31	DP_LN1_TXN
			P97	S98	DP0_HPD_EXT	AB33	DPTX_HPD
HDMITX21_CH0_P	AN35	HDMI_D0+	P98	S99	DP0_LANE2+	AJ34	DP_LN2_TXP
HDMITX21_CH0_M	AN34	HDMI_D0-	P99	S100	DP0_LANE2-	AJ33	DP_LN2_TXN
			P100	S101			
HDMITX21_CLK_P	AR34	HDMI_CK+	P101	S102	DP0_LANE3+	AK32	DP_LN3_TXP
HDMITX21_CLK_M	AR35	HDMI_CK-	P102	S103	DP0_LANE3-	AK31	DP_LN3_TXN
			P103	S104			

HDMITX_HTPLG	AC32	HDMI_HPD	P104	S105	DP0_AUX+	AJ36	DPAUXP
HDMITX_SCL	AD32	HDMI_CTRL_CK	P105	S106	DP0_AUX-	AJ37	DPAUXN
HDMITX_SDA	AD33	HDMI_CTRL_DAT	P106	S107	LCD1_BKLT_EN	AA11	DSI1_LCM_RST
			P107	S108			
CMMPDN0	G4	GPIO0/CAM0_PWR#	P108	S109			
CMMPDN1	E3	GPIO1/CAM1_PWR#	P109	S110			
CMMRST0	G3	GPIO2/CAM0_RST#	P110	S111			
CMMRST1	G5	GPIO3/CAM1_RST#	P111	S112			
			P112	S113	EDP1_HPD_EXT	AA35	GPIO17
			P113	S114			
GPIO00	Y10	GPIO6	P114	S115			
GPIO09	V4	GPIO7	P115	S116	LVDS1_VDD_EN	Y5	DSI1_DSI_TE
GPIO10	V5	GPIO8	P116	S117			
GPIO11	W8	GPIO9	P117	S118			
GPIO01	U10	GPIO10	P118	S119			
			P119	S120			
			P120	S121			
SCL3	W2	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	Y11	DISP_PWM1
SDA3	W1	I2C_PM_DAT	P122	S123			
			P123	S124			
			P124	S125			
			P125	S126			
			P126	S127	LCD0_BKLT_EN	Y9	DSI0_LCM_RST
			P127	S128			
			P128	S129			
UART1_TXD	V1	SER0_TX	P129	S130			
UART1_RXD	V2	SER0_RX	P130	S131			
UART2_TXD	U4	SER0_RTS#	P131	S132			
UART2_RXD	U5	SER0_CTS#	P132	S133	LCD0_VDD_EN	AA7	DSI0_DSI_TE

			P133	S134			
UART0_TXD	U2	SER1_TX	P134	S135			
UART0_RXD	U3	SER1_RX	P135	S136			
SPIM2_CSB*	G2	SER2_TX	P136	S137			
SPIM2_CLK*	G1	SER2_RX	P137	S138			
SPIM2_MOSI*	F2	SER2_RTS#	P138	S139	I2C_LCD_CK	Y4	SCL0
SPIM2_MISO*	E2	SER2_CTS#	P139	S140	I2C_LCD_DAT	W6	SDA0
DPI_DE	AB2	SER3_TX	P140	S141	LCD0_BKLT_PWM	AA9	DISP_PWMO
DPI_CK	AB1	SER3_RX	P141	S142			
			P142	S143			
			P143	S144			
			P144	S145			
			P145	S146	PCIE_WAKE#	AA4	PCIE_WAKE_N
			P146	S147			
			P147	S148			
			P148	S149			
			P149	S150			
			P150	S151			
			P151	S152			
			P152	S153			
			P153	S154			
			P154	S155			
			P155	S156			
			P156	S157			
				S158			

* These four signals are only available if they are not required for the WiFi module

4.2 Thermal Design

Highly integrated modules like SOM-SMARC-GENIO offer very high performance within small dimensions. On the other hand, the miniaturization of ICs and the high operating frequencies of the processors lead to high heat generation that must be dissipated in order to maintain the CPU within its allowed temperature range.

The operating temperature specified in the Technical Features of SOM-SMARC-GENIO module indicates the temperature range in which any and all parts of the heat spreader / heat sink must remain, in order for SECO to guarantee functionality. Hence, these numbers do not necessarily indicate the suitable environmental temperature.

The heat spreader is not intended to be a guaranteed standalone cooling system, but should be used only as a supplemental means of transferring heat to another dissipation system (i.e. heat sinks, fans, heat pipes etc).

It is the customer's responsibility to design and apply an application-dependent cooling system, capable of ensuring that the heat spreader / heat sink temperature remain within the indicated range of the module.

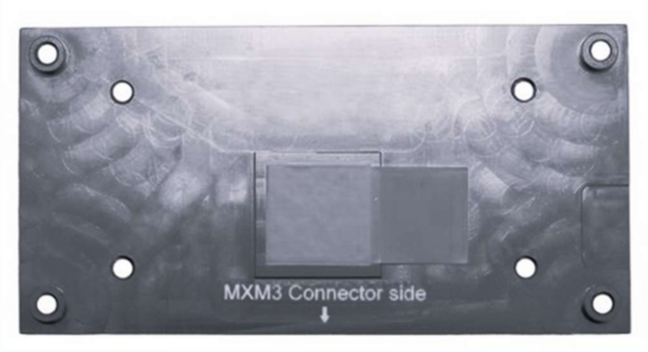
It is an absolute requirement that the customer, after thorough evaluation of the processor's workload in the actual system application, the system enclosure and consequent air flow/Thermal analysis, accurately study and develop a suitable cooling solution for the assembled system.

SECO can provide SOM-SMARC-GENIO module specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

SMARC® HEAT SPREADER

(Sample)

Bottom view



Top view

Ordering Code	Description
DM02-00005A	SMARC® HEAT SPREADER: Heat Spreader SOM-SMARCs GENIO (PASSIVE) - Packaged
DT01-00006A	Thermal Gap Filler : Thermal Gap Filler 1,0mm 5W/mK
DT01-00007A	Thermal Gap Filler : Thermal Gap Filler 1,5mm 5.0W/mK

Warning!

The thermal solutions available with SECO boards are tested in the commercial temperature range (0-60°C), without housing and inside climatic chamber. Therefore, the customer is suggested to study, develop and validate the cooling solution for his system, considering ambient temperature, processor's workload, utilisation scenarios, enclosures, air flow and so on.

In particular, the heatspreader is not intended to be a cooling system by itself, but only as the standard means for transferring heat to cooler, like heatsinks, cold plate, heat pipes and so on.

4.3 What's different in Rev.A / Rev.B ?

4.3.1 Boot Select

The following signals are active low and driven by open drain circuitry on the carrier board.

BOOT_SEL0#: Boot Device Selection #0. Input, +1.8V_ALW electrical level with a 10kΩ pull-up resistor
BOOT_SEL1#: Boot Device Selection #1. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor
BOOT_SEL2#: Boot Device Selection #2. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor
FORCE_RECOV#: Force recovery Mode. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor

SMARC® Golden Finger Connector

TOP SIDE				BOTTOM SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
				S1	I2C6_SCL	O	I2C
MANAGEMENT	I	SMB_ALERT_1V8#	P1	S2	I2C6_SDA	I/O	I2C
		GND	P2	S3	GND		
CAMERA	I	CSI1_CK+	P3	S4	N.C.		
CAMERA	I	CSI1_CK-	P4	S5	I2C5_SCL	O	I2C
		N.C.	P5	S6	CAM_MCK	O	CAMERA
		N.C.	P6	S7	I2C5_SDA	I/O	I2C
CAMERA	I	CSI1_RX0+	P7	S8	CSI0_CK+	I	CAMERA
CAMERA	I	CSI1_RX0-	P8	S9	CSI0_CK-	I	CAMERA
		GND	P9	S10	GND		
CAMERA	I	CSI1_RX1+	P10	S11	CSI0_RX0+	I	CAMERA
CAMERA	I	CSI1_RX1-	P11	S12	CSI0_RX0-	I	CAMERA

		GND	P12	S13	GND		
CAMERA	I	CSI1_RX2+	P13	S14	CSI0_RX1+	I	CAMERA
CAMERA	I	CSI1_RX2-	P14	S15	CSI0_RX1-	I	CAMERA
		GND	P15	S16	GND		
CAMERA	I	CSI1_RX3+	P16	S17	GBE1_MDI0+	I/O	GBE
CAMERA	I	CSI1_RX3-	P17	S18	GBE1_MDI0-	I/O	GBE
		GND	P18	S19	GBE1_LINK100#	O	GBE
GBE	I/O	GBE0_MDI3-	P19	S20	GBE1_MDI1+	I/O	GBE
GBE	I/O	GBE0_MDI3+	P20	S21	GBE1_MDI1-	I/O	GBE
GBE	O	GBE0_LINK100#	P21	S22	N.C.		
GBE	O	GBE0_LINK1000#	P22	S23	N.C.		
GBE	I/O	GBE0_MDI2-	P23	S24	N.C.		
GBE	I/O	GBE0_MDI2+	P24	S25	GND		
GBE	O	GBE0_LINK_ACT#	P25	S26	N.C.		
GBE	I/O	GBE0_MDI1-	P26	S27	N.C.		
GBE	I/O	GBE0_MDI1+	P27	S28	USB_VDD33A		
		N.C.	P28	S29	N.C.		
GBE	I/O	GBE0_MDI0-	P29	S30	N.C.		
GBE	I/O	GBE0_MDI0+	P30	S31	GBE1_LINK_ACT#	O	GBE
		N.C.	P31	S32	N.C.		
		GND	P32	S33	N.C.		
		N.C.	P33	S34	GND		
SDIO_CARD	I/O	SDIO_CMD	P34	S35	USB4+	I/O	USB
SDIO_CARD	I	SDIO_CD#	P35	S36	USB4-	I/O	USB
SDIO_CARD	O	SDIO_CK	P36	S37	N.C.		
SDIO_CARD	O	SDIO_PWR_EN	P37	S38	I2S0_MCK	O	AUDIO
		GND	P38	S39	I2S0_LRCK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D0	P39	S40	I2S0_SDOUT	O	AUDIO
SDIO_CARD	I/O	SDIO_D1	P40	S41	I2S0_SDIN	I	AUDIO

SDIO_CARD	I/O	SDIO_D2	P41	S42	I2S0_CK	O	AUDIO
SDIO_CARD	I/O	SDIO_D3	P42	S43	N.C.		
SPI_INTERFACE	O	SPI0_CS0#	P43	S44	N.C.		
SPI_INTERFACE	O	SPI0_CK	P44	S45	N.C.		
SPI_INTERFACE	I	SPI0_DIN	P45	S46	N.C.		
SPI_INTERFACE	O	SPI0_DO	P46	S47	GND		
		GND	P47	S48	I2C_GP_CK	I/O	I2C
		N.C.	P48	S49	I2C_GP_DAT	I/O	I2C
		N.C.	P49	S50	I2S2_LRCK	I/O	AUDIO
		GND	P50	S51	I2S2_SDOUT	O	AUDIO
		N.C.	P51	S52	I2S2_SDIN	I	AUDIO
		N.C.	P52	S53	I2S2_CK	O	AUDIO
		GND	P53	S54	N.C.		
SPI_INTERFACE	O	ESPI_CS0#	P54	S55	USB5_EN_OC#	I/O	USB
		N.C.	P55	S56	ESPI_IO_2	I/O	SPI_INTERFACE
SPI_INTERFACE	O	ESPI_CK	P56	S57	ESPI_IO_3	I/O	SPI_INTERFACE
SPI_INTERFACE	I/O	ESPI_IO_1	P57	S58	N.C.		
SPI_INTERFACE	I/O	ESPI_IO_0	P58	S59	USB5+	I/O	USB
		GND	P59	S60	USB5-		USB
USB	I/O	USB0+	P60	S61	GND		
USB	I/O	USB0-	P61	S62	N.C.		
USB	I/O	USB0_EN_OC#	P62	S63	N.C.		
USB	I	USB0_VBUS_DET	P63	S64	GND		
USB	I	USB0_OTG_ID	P64	S65	N.C.		
USB	I/O	USB1+	P65	S66	N.C.		
USB	I/O	USB1-	P66	S67	GND		
USB	I/O	USB1_EN_OC#	P67	S68	USB3+	I/O	USB
		GND	P68	S69	USB3-	I/O	USB
USB	I/O	USB2+	P69	S70	GND		

USB	I/O	USB2-	P70	S71	USB2_SSTX+	O	USB
USB	I/O	USB2_EN_OC#	P71	S72	USB2_SSTX-	O	USB
STM32		STM32_RST#	P72	S73	GND		
		N.C	P73	S74	USB2_SSRX+	I	USB
USB	I/O	USB3_EN_OC#	P74	S75	USB2_SSRX-	I	USB
PCI_e	O	PCIE_A_RST#	P75	S76	N.C.		
USB	I/O	USB4_EN_OC#	P76	S77	N.C.		
PCI_e	I/O	PCIE_B_CKREQ#	P77	S78	N.C.		
PCI_e	I/O	PCIE_A_CKREQ#	P78	S79	N.C.		
		GND	P79	S80	GND		
		N.C.	P80	S81	N.C.		
		N.C.	P81	S82	N.C.		
		GND	P82	S83	GND		
PCI_e	O	PCIE_A_REFCK+	P83	S84	N.C.		
PCI_e	O	PCIE_A_REFCK-	P84	S85	N.C.		
		GND	P85	S86	GND		
PCI_e	I	PCIE_A_RX+	P86	S87	N.C.		
PCI_e	I	PCIE_A_RX-	P87	S88	N.C.		
		GND	P88	S89	GND		
PCI_e	O	PCIE_A_TX+	P89	S90	N.C.		
PCI_e	O	PCIE_A_TX-	P90	S91	N.C.		
		GND	P91	S92	GND		
SECONDARY_DISPLAY	O	HDMI_D2+	P92	S93	DP0_LANE0+	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_D2-	P93	S94	DP0_LANE0-	O	PRIMARY_DISPLAY
		GND	P94	S95	DP0_AUX_SEL	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_D1+	P95	S96	DP0_LANE1+	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_D1-	P96	S97	DP0_LANE1-	O	PRIMARY_DISPLAY
		GND	P97	S98	DP0_HPD_EXT	I	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_D0+	P98	S99	DP0_LANE2+	O	PRIMARY_DISPLAY

SECONDARY_DISPLAY	O	HDMI_D0-	P99	S100	DP0_LANE2-	O	PRIMARY_DISPLAY
		GND	P100	S101	GND		
SECONDARY_DISPLAY	O	HDMI_CK+	P101	S102	DP0_LANE3+	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	O	HDMI_CK-	P102	S103	DP0_LANE3-	O	PRIMARY_DISPLAY
		GND	P103	S104	N.C.		
SECONDARY_DISPLAY	I	HDMI_HPD	P104	S105	DP0_AUX+	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	I/O	HDMI_CTRL_CK	P105	S106	DP0_AUX-	O	PRIMARY_DISPLAY
SECONDARY_DISPLAY	I/O	HDMI_CTRL_DAT	P106	S107	LCD1_BKLT_EN	O	LCD_SUPPORT
		DP1_AUX_SEL	P107	S108	LVDS1_EDP_CK+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO0 / CAM0_PWR#	P108	S109	LVDS1_EDP_CK-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO1 / CAM1_PWR#	P109	S110	GND		
GPIO	I/O	GPIO2 / CAM0_RST#	P110	S111	LVDS1_EDP_0+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO3 / CAM1_RST#	P111	S112	LVDS1_EDP_0-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO4	P112	S113	EDP1_HPD_EXT		
GPIO	I/O	GPIO5	P113	S114	LVDS1_EDP_1+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO6	P114	S115	LVDS1_EDP_1-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO7	P115	S116	LCD1_VDD_EN	O	LCD_SUPPORT
GPIO	I/O	GPIO8	P116	S117	LVDS1_2+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO9	P117	S118	LVDS1_2-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO10	P118	S119	GND		
GPIO	I/O	GPIO11	P119	S120	LVDS1_3+	O	PRIMARY_DISPLAY
		GND	P120	S121	LVDS1_3-	O	PRIMARY_DISPLAY
MANAGEMENT	I/O	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	O	LCD_SUPPORT
MANAGEMENT	I/O	I2C_PM_DAT	P122	S123	GPIO13	I/O	GPIO
BOOT_SEL	I	BOOT_SEL0#	P123	S124	GND		
BOOT_SEL	I	BOOT_SEL1#	P124	S125	LVDS0_TX0+	O	PRIMARY_DISPLAY
BOOT_SEL	I	BOOT_SEL2#	P125	S126	LVDS0_TX0-	O	PRIMARY_DISPLAY
MANAGEMENT	O	RESET_OUT#	P126	S127	LCD0_BKLT_EN	O	LCD_SUPPORT
MANAGEMENT	I	RESET_IN#	P127	S128	LVDS0_TX1+	O	PRIMARY_DISPLAY

MANAGEMENT	I	POWER_BTN#	P128	S129	LVDS0_TX1-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_TX	P129	S130	GND		
ASYNC_SERIAL	I	SER0_RX	P130	S131	LVDS0_TX2+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_RTS#	P131	S132	LVDS0_TX2-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER0_CTS#	P132	S133	LCD0_VDD_EN	O	LCD_SUPPORT
		GND	P133	S134	LVDS0_CK+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER1_TX	P134	S135	LVDS0_CK-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER1_RX	P135	S136	GND		
ASYNC_SERIAL	O	SER2_TX	P136	S137	LVDS0_TX3+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER2_RX	P137	S138	LVDS0_TX3-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER2_RTS#	P138	S139	I2C0_SCL	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER2_CTS#	P139	S140	I2C0_SDA	I/O	LCD_SUPPORT
ASYNC_SERIAL	O	SER3_TX	P140	S141	LCD0_BKLT_PWM	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER3_RX	P141	S142	GPIO12	I/O	GPIO
		GND	P142	S143	GND		
CAN	O	CAN0_TX	P143	S144	eDP0_HPD	I	PRIMARY_DISPLAY
CAN	I	CAN0_RX	P144	S145	WDT_TIME_OUT#	O	WATCHDOG
		N.C.	P145	S146	PCIE_WAKE#	I	PCI_e
		N.C.	P146	S147	VDD_RTC		
		VDD_IN	P147	S148	LID#	I	MANAGEMENT
		VDD_IN	P148	S149	SLEEP#	I	MANAGEMENT
		VDD_IN	P149	S150	VIN_PWR_BAD#	I	MANAGEMENT
		VDD_IN	P150	S151	CHARGING#	I	MANAGEMENT
		VDD_IN	P151	S152	CHARGER_PRSNT#	I	MANAGEMENT
		VDD_IN	P152	S153	CARRIER_STBY#	O	MANAGEMENT
		VDD_IN	P153	S154	CARRIER_PWR_ON	O	MANAGEMENT
		VDD_IN	P154	S155	FORCE_RECOV#	I	BOOT_SEL
		VDD_IN	P155	S156	BATLOW#	I	MANAGEMENT
		VDD_IN	P156	S157	TEST#	I	MANAGEMENT

S158	GND

4.3.2 Management pins

According to the SMARC® specifications, the input pins listed below are all Active Low, meant to be driven by open drain devices on the carrier board:

VIN_PWR_BAD#: Power Bad indication signal from the Carrier Board
CARRIER_PWR_ON: Power On. Command to the Carrier Board. Output, +1.8V_ALW electrical level
CARRIER_STBY#: Stand By command to the Carrier Board. Output, +1.8V_ALW electrical level
RESET_OUT#: General Purpose Reset. Output, +1.8V_ALW electrical level
RESET_IN#: General Purpose Reset. Input, +3.3V_ALW electrical level
POWER_BTN#: Power Button. Input, +3.3V_ALW electrical level
SLEEP#: Sleep indicator from Carrier board. Input, +1.8V_ALW electrical level (Standby not supported)
LID#: LID Switch. Input, +3.3V_ALW electrical level
BATLOW#: Battery Low indication signal from the Carrier Board. Input, +3.3V_ALW electrical level
CHARGING#: Battery Charging Input Signal from the Carrier Board. Input, +3.3V_ALW electrical level
CHARGER_PRSNT#: Battery Charger Present input from the Carrier Board. Input, +3.3V_ALW electrical level
TEST#: Held low by Carrier to invoke Module vendor specific test function(s). Input. +3.3V_ALW electrical level with a 10kΩ pull-up resistor
SMB_ALERT_1V8#: SM Bus Alert# (interrupt) signal. Input, +1.8V_ALW electrical level with a 2k2Ω pull-up resistor

4.3.3 Boot Select

The following signals are active low and driven by open drain circuitry on the carrier board.

BOOT_SEL0#: Boot Device Selection #0. Input, +1.8V_ALW electrical level with a 10kΩ pull-up resistor
BOOT_SEL1#: Boot Device Selection #1. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor
BOOT_SEL2#: Boot Device Selection #2. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor
FORCE_RECOV#: Force recovery Mode. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor

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