# Myon I

Documentation version 1.9

## Introduction

The Myon I is the first module in a series of modules using the Myon SOM standard.

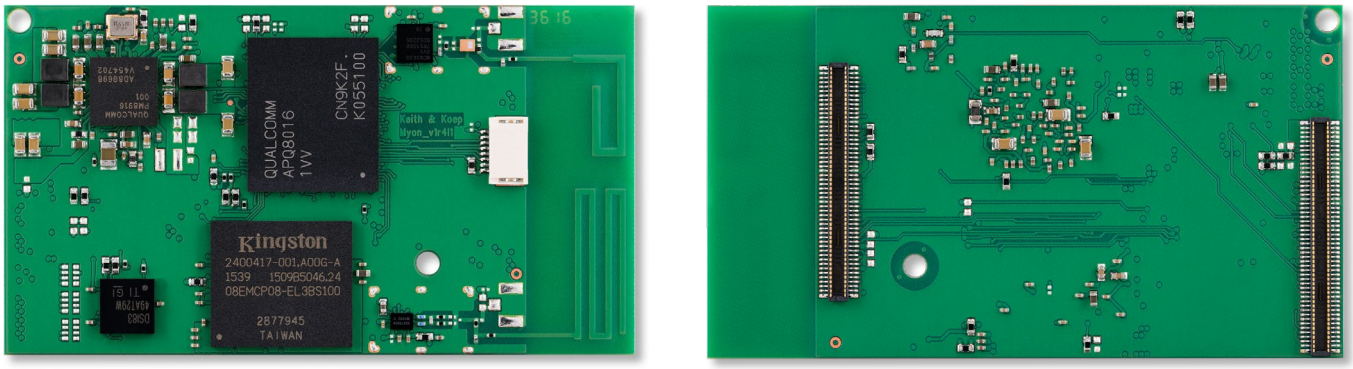
It is powered by a 64-bit Qualcomm Snapdragon 410E Quad-core Arm® Cortex A53 processor and features all things needed to build a complete and small solution. Power-Management, Battery-Charger, Storage-Memory, RAM, LVDS-Transceiver, Audio, Wireless-LAN, Bluetooth and GPS are already integrated on the module and only a single power-source is needed to have a fully functional system.

Additional peripherals may be added through two 100pin Hirose DF40 connectors.
The IO-Ports use a voltage level of 1.8V.

There are two main mounting options:
- UFL-Antenna Connectors or On-Board Antennas.
- LVDS or Mipi Display Interface.

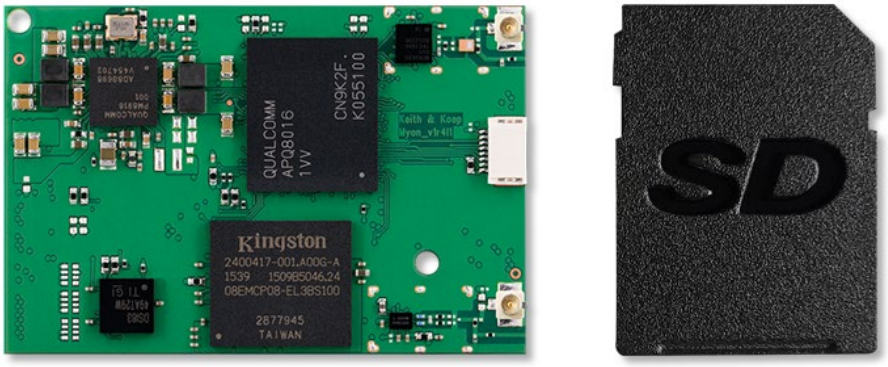
## Wireless-Version (with On-Board Antennas)

Version with LVDS Display interface, size 58 x 32 x 4.2 mm, front and back




## Wireless-Version (external Antennas)

Version with LVDS Display interface, size 48 x 32 x 4.2 mm (size of 2 SD-Cards),
size comparison with SD-Card



# Simplified Block Diagram of Myon I

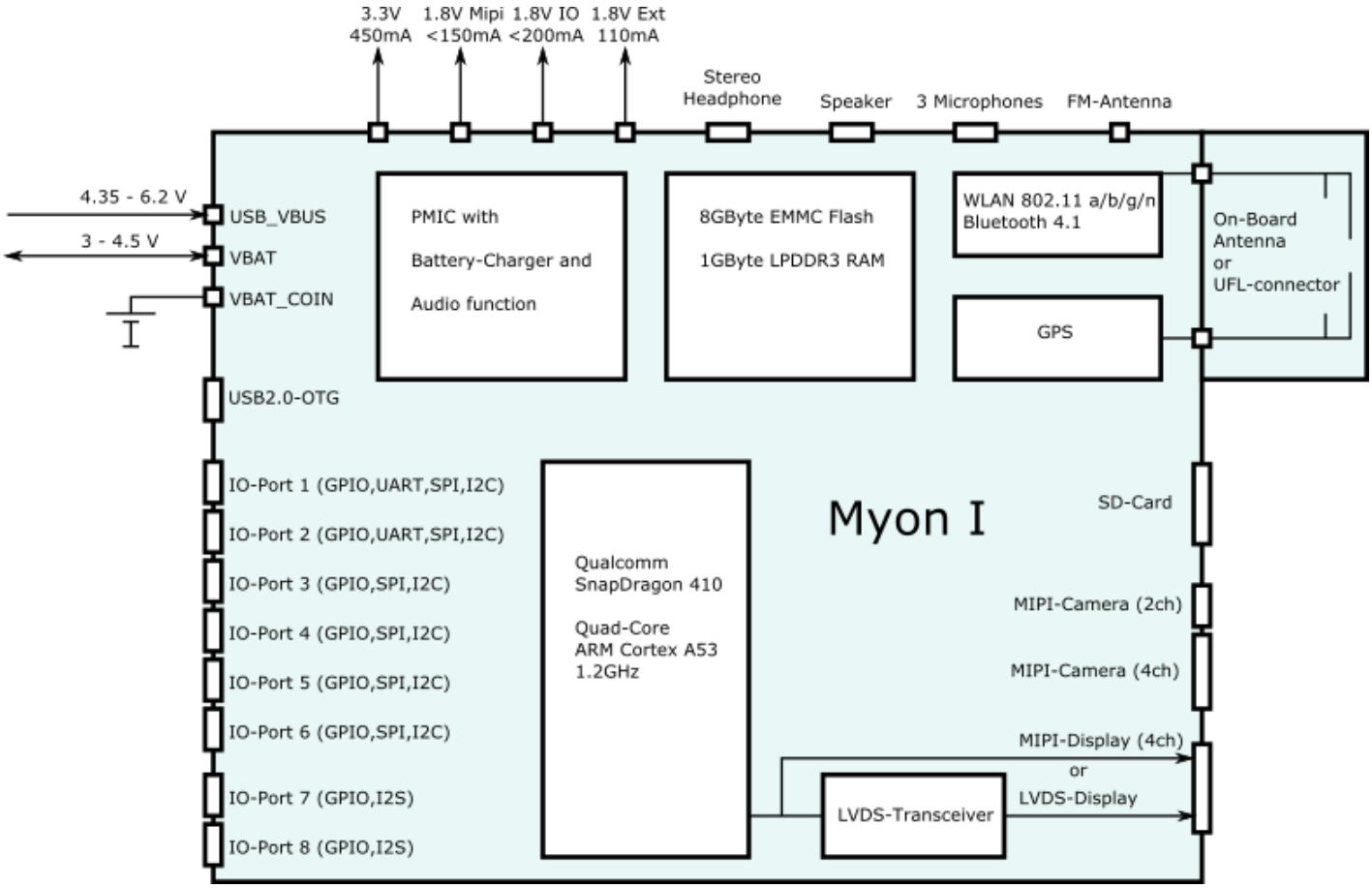



Figure 0-1

# Features and Interfaces

## Features

**Processor:**
Qualcomm Snapdragon 410E Quad-core ARM® Cortex A53 at up to 1.2GHz
Qualcomm Adreno 306 400MHz GPU including support for OpenGL ES 3.0, OpenCL and DirectX.

**Memory:**
1 GByte LPDDR3 533MHz

**Storage:**
8 GByte eMMC 4.51

**Wireless:**
WLAN 802.11 a/b/g/n 2.4GHz
Bluetooth 4.1
On-Board Antennas or UFL-connector

**Power:**
PMIC to generate internal and external voltages.
Lithium-ion, lithium-ion-polymer battery-charger
Coin-Cell Charger (lithium manganese dioxide rechargeable coin cell or keep-alive capacitor)

**Dimensions:**
Without Antenna (Length x Width x Height): 48 x 32 x 4.2 mm
With Antenna (Length x Width x Height): 58 x 32 x 4.2 mm

Overall height from your baseboard to the upper edge of the Myon I depend on the connector-receptible used and is either 4.5 or 7 mm.

## Interfaces / Signals accessible over extension connectors

- Power Supply through +5V or +3.3V or Battery.
- Regulated 1.8V and 3.3V outputs.
- USB2.0 OTG port (USB Host or Slave).
- SD/SDIO Card Interface
- 8 IO-Ports configurable for different interfaces: GPIO, UART, SPI, I2C, I2S
- Mipi Camera (2ch) and Mipi Camera (4ch) interface.
- Mipi Display (4ch) or LVDS Display interface.
- Stereo Headphone output.
- Mono Speaker 8Ω.
- 3 Microphone inputs
- FM-Antenna pin.
- \RESET_OUT, \RESET_IN and other Control-Signals

# 1 Pin-Description

The Myon I got two Hirose DF40C-100DP-0.4V pin-headers **J70** and **J71**.
These can be mated with following receptibles:
DF40C-100DS-0.4V (1.5mm stack height)
DF40C-3.0-100DS-0.4V (3.0mm stack height)

All signals needed for operation are placed on the main connector **J70**.

**J74**: JTAG connector.
**J40**: UFL connector for WLAN and Bluetooth.
**J41**: UFL connector for GPS.

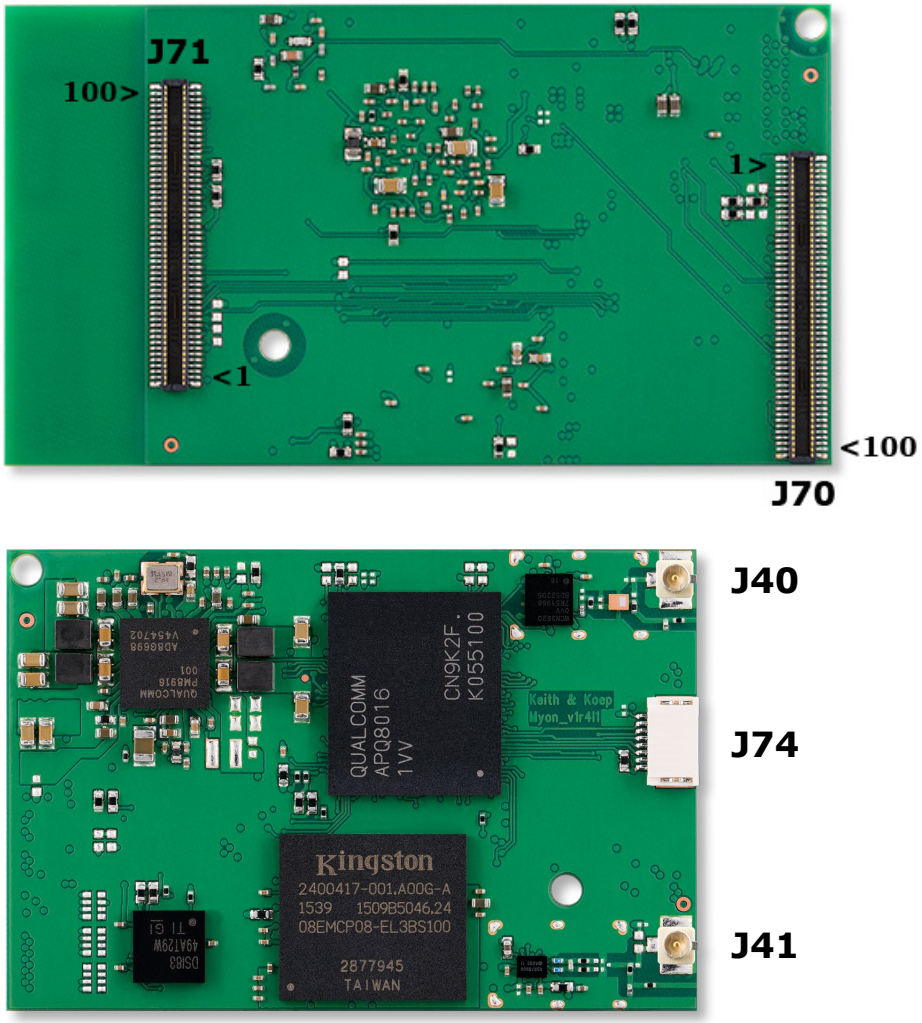



Figure 1-1: Connectors

## 1.1 Pin-Description (Primary Function)

Pins not assigned to a signal are not connected on Myon I and are reserved for future use. Do not connect.

(See next page for tables)

## J70: Main Connector

| Signal | Pin | | Pin | Signal |
|---|---|---|---|---|
| VBAT | 1 | | 2 | VBAT |
| VBAT | 3 | | 4 | VBAT |
| VBAT | 5 | | 6 | VBAT |
| VBAT | 7 | | 8 | VBAT |
| BAT_THERM | 9 | | 10 | BAT_SENSE |
| VBAT_COIN | 11 | | 12 | BAT_ID |
| GND | 13 | | 14 | GND |
| GND | 15 | | 16 | GND |
| USB_VBUS | 17 | | 18 | USB_VBUS |
| USB_VBUS | 19 | | 20 | USB_VBUS |
| USB_VBUS | 21 | | 22 | USB_VBUS |
| USB_VBUS | 23 | | 24 | USB_VBUS |
| USB_OTG_VBUS | 25 | | 26 | USB_VBUS |
| USB_OTG_DM | 27 | | 28 | PHONE_ON_N |
| USB_OTG_DP | 29 | | 30 | RESET_IN_N |
| USB_OTG_ID | 31 | | 32 | RESET_OUT_N |
| GND | 33 | | 34 | GND |
| GND_CFILT | 35 | | 36 | GND |
| MIC2 | 37 | | 38 | JTAG_MODE |
| MIC_BIAS2 | 39 | | 40 | FORCE_USB_BOOT |
| HEADPHONE_L | 41 | | 42 | +3V3 |
| HEADPHONE_R | 43 | | 44 | +3V3 |
| HEADPHONE_REF | 45 | | 46 | +1V8_MIPI |
| HEADSET_DETECT | 47 | | 48 | +1V8_MIPI |
| MIC1 | 49 | | 50 | +1V8_EXT |
| MIC_BIAS1 | 51 | | 52 | +1V8_IO |
| FM_ANTENNA | 53 | | 54 | P3_MOSI |
| MIC3 | 55 | | 56 | P3_MISO |
| SPEAKER_P | 57 | | 58 | P3_CLK_SCL |
| SPEAKER_N | 59 | | 60 | P3_CS_SDA |
| P1_TXD_MOSI | 61 | | 62 | P4_MOSI |
| P1_RXD_MISO | 63 | | 64 | P4_MISO |
| P1_RTS_CLK_SCL | 65 | | 66 | P4_CLK_SCL |
| P1_CTS_CS_SDA | 67 | | 68 | P4_CS_SDA |
| P2_TXD_MOSI | 69 | | 70 | DSI0_RESET |
| P2_RXD_MISO | 71 | | 72 | DSI0_ENABLE |
| P2_RTS_CLK_SCL | 73 | | 74 | BACKLIGHT_PWM |
| P2_CTS_CS_SDA | 75 | | 76 | BACKLIGHT_ENABLE |
| GND | 77 | | 78 | GND |
| VDD_SDCARD_PWR | 79 | | 80 | DSI0_DAT0_N / LVDS_TXN0 |
| VDD_SDCARD_IO | 81 | | 82 | DSI0_DAT0_P / LVDS_TXP0 |
| SD2_CMD | 83 | | 84 | DSI0_DAT1_N / LVDS_TXN1 |
| SD2_CLK | 85 | | 86 | DSI0_DAT1_P / LVDS_TXP1 |
| SD2_DAT0 | 87 | | 88 | DSI0_DAT2_N / LVDS_TXN2 |
| SD2_DAT1 | 89 | | 90 | DSI0_DAT2_P / LVDS_TXP2 |
| SD2_DAT2 | 91 | | 92 | DSI0_DAT3_N / LVDS_TXN3 |
| SD2_DAT3 | 93 | | 94 | DSI0_DAT3_P / LVDS_TXP3 |
| SD2_CARDDETECT_N | 95 | | 96 | DSI0_CLK_N / LVDS_CLKN |
| SD2_WRITEPROTECT | 97 | | 98 | DSI0_CLK_P / LVDS_CLKP |
| GND | 99 | | 100 | GND |

## J71: Aux Connector

| Signal | Pin | | Pin | Signal |
|---|---|---|---|---|
| BOOT_CONFIG_1 | 1 | | 2 | WLAN_LED |
| BBCLK2 | 3 | | 4 | BT_LED |
| HDMI_INT | 5 | | 6 | KYPD_SNS0 |
| P5_MOSI | 7 | | 8 | KYPD_SNS1 |
| P5_MISO | 9 | | 10 | KYPD_SNS2 |
| P5_CLK_SCL | 11 | | 12 | USR_LED2 |
| P5_CS_SDA | 13 | | 14 | USR_LED3 |
| P6_MOSI | 15 | | 16 | USR_LED4 |
| P6_MISO | 17 | | 18 | USB_HUB_RESET_N |
| P6_CLK_SCL | 19 | | 20 | USB_SW_SEL |
| P6_CS_SDA | 21 | | 22 | |
| I2S1_DAT0 | 23 | | 24 | |
| I2S1_DAT1 | 25 | | 26 | |
| I2S1_SCK | 27 | | 28 | |
| I2S1_MCLK | 29 | | 30 | |
| I2S1_WS | 31 | | 32 | |
| I2S2_DAT0 | 33 | | 34 | |
| I2S2_DAT1 | 35 | | 36 | |
| I2S2_SCK | 37 | | 38 | |
| I2S2_WS | 39 | | 40 | |
| GND | 41 | | 42 | GND |
| CSI1_CLK_N | 43 | | 44 | |
| CSI1_CLK_P | 45 | | 46 | |
| CSI1_DAT0_N | 47 | | 48 | |
| CSI1_DAT0_P | 49 | | 50 | |
| CSI1_DAT1_N | 51 | | 52 | |
| CSI1_DAT1_P | 53 | | 54 | |
| GND | 55 | | 56 | GND |
| CSI1_RESET | 57 | | 58 | |
| CSI1_PWDN | 59 | | 60 | |
| CSI1_MCLK | 61 | | 62 | GPIO78 |
| CAM_TORCH | 63 | | 64 | GPIO79 |
| CAM_FLASH | 65 | | 66 | GPIO95 |
| CAM_I2C_SCL | 67 | | 68 | GPIO99 |
| CAM_I2C_SDA | 69 | | 70 | GPIO100 |
| CSI0_RESET | 71 | | 72 | GPIO101 |
| CSI0_PWDN | 73 | | 74 | GPIO102 |
| CSI0_MCLK | 75 | | 76 | GPIO103 |
| GND | 77 | | 78 | GND |
| CSI0_CLK_N | 79 | | 80 | |
| CSI0_CLK_P | 81 | | 82 | GPIO59 |
| CSI0_DAT0_N | 83 | | 84 | GPIO60 |
| CSI0_DAT0_P | 85 | | 86 | GPIO58 |
| CSI0_DAT1_N | 87 | | 88 | GPIO57 |
| CSI0_DAT1_P | 89 | | 90 | GPIO61 |
| CSI0_DAT2_N | 91 | | 92 | GPIO62 |
| CSI0_DAT2_P | 93 | | 94 | GPIO105 |
| CSI0_DAT3_N | 95 | | 96 | GPIO106 |
| CSI0_DAT3_P | 97 | | 98 | GPIO96 |
| GND | 99 | | 100 | GND |

### J74: JTAG Connector

This flex-cable-connector uses the Keith-Koep Jtag connector standard. An Adapter to Multi-ICE pin-header is available.

| Pin | Signal |
|---|---|
| 1 | +1V8_IO |
| 2 | GND |
| 3 | JTAG_TMS |
| 4 | JTAG_TRST_N |
| 5 | JTAG_TCK |
| 6 | JTAG_TDO |
| 7 | JTAG_TDI |
| 8 | JTAG_SRST_N |

## 1.2 Pin-Mux Information

Several pins are GPIOs which may be configured for different functions by software. Please check with the processor datasheet for additional pin-mux information.

| PIN | Name | Mux1 | Mux2 | Mux3 | Mux4 |
|---|---|---|---|---|---|
| J70-61 | P1_TXD_MOSI | GPIO0 | UART1_TXD | SPI1_MOSI | |
| J70-63 | P1_RXD_MISO | GPIO1 | UART1_RXD | SPI1_MISO | |
| J70-65 | P1_RTS_CLK_SCL | GPIO3 | UART1_RTS | SPI1_CLK | I2C1_SCL |
| J70-67 | P1_CTS_CS_SDA | GPIO2 | UART1_CTS | SPI1_CS | I2C1_SDA |
| J70-69 | P2_TXD_MOSI | GPIO4 | UART2_TXD | SPI2_MOSI | |
| J70-71 | P2_RXD_MISO | GPIO5 | UART2_RXD | SPI2_MISO | |
| J70-73 | P2_RTS_CLK_SCL | GPIO7 | UART2_RTS | SPI2_CLK | I2C2_SCL |
| J70-75 | P2_CTS_CS_SDA | GPIO6 | UART2_CTS | SPI2_CS | I2C2_SDA |
| J70-54 | P3_MOSI | GPIO8 | | SPI3_MOSI | |
| J70-56 | P3_MISO | GPIO9 | | SPI3_MISO | |
| J70-58 | P3_CLK_SCL | GPIO11 | | SPI3_CLK | I2C3_SCL |
| J70-60 | P3_CS_SDA | GPIO10 | | SPI3_CS | I2C3_SDA |
| J70-62 | P4_MOSI | GPIO12 | | SPI4_MOSI | |
| J70-64 | P4_MISO | GPIO13 | | SPI4_MISO | |
| J70-66 | P4_CLK_SCL | GPIO15 | | SPI4_CLK | I2C4_SCL |
| J70-68 | P4_CS_SDA | GPIO14 | | SPI4_CS | I2C4_SDA |
| J71-7 | P5_MOSI | GPIO16 | | SPI5_MOSI | |
| J71-9 | P5_MISO | GPIO17 | | SPI5_MISO | |
| J71-11 | P5_CLK_SCL | GPIO19 | | SPI5_CLK | I2C5_SCL |
| J71-13 | P5_CS_SDA | GPIO18 | | SPI5_CS | I2C5_SDA |
| J71-15 | P6_MOSI | GPIO20 | | SPI6_MOSI | |
| J71-17 | P6_MISO | GPIO21 | | SPI6_MISO | |
| J71-19 | P6_CLK_SCL | GPIO23 | | SPI6_CLK | I2C6_SCL |
| J71-21 | P6_CS_SDA | GPIO22 | | SPI6_CS | I2C6_SDA |
| J71-23 | I2S1_DAT0 | GPIO114 | MI2S_1_D0 | | |
| J71-25 | I2S1_DAT1 | GPIO115 | MI2S_1_D1 | GYRO_ACCEL_INT | |
| J71-27 | I2S1_SCK | GPIO113 | MI2S_1_SCLK | | GP_PDM_2B |
| J71-29 | I2S1_MCLK | GPIO116 | MI2S_1_MCLK | | |
| J71-31 | I2S1_WS | GPIO110 | MI2S_1_WS | SPI1_CS1 | GP_MN |

| PIN | Name | Mux1 | Mux2 | Mux3 | Mux4 |
|---|---|---|---|---|---|
| J71-33 | I2S2_DAT0 | GPIO119 | MI2S_2_D0 | | |
| J71-35 | I2S2_DAT1 | GPIO112 | MI2S_2_D1 | | |
| J71-37 | I2S2_SCK | GPIO118 | MI2S_2_SCLK | | |
| J71-39 | I2S2_WS | GPIO117 | MI2S_2_WS | | |
| J71-63 | CAM_TORCH | GPIO24 | MDP_VSYNC | | |
| J71-65 | CAM_FLASH | GPIO36 | FLASH_LED_RESET | | |
| J71-69 | CAM_I2C_SDA | GPIO29 | CAM_I2C_SDA | | |
| J71-67 | CAM_I2C_SCL | GPIO30 | CAM_I2C_SCL | | |
| J71-75 | CSI0_MCLK | GPIO26 | CAM_MCLK0 | | |
| J71-73 | CSI0_PWDN | GPIO34 | CAM0_STBY | | |
| J71-71 | CSI0_RESET | GPIO35 | CAM0_RST | | |
| J71-61 | CSI1_MCLK | GPIO27 | CAM_MCLK1 | | |
| J71-59 | CSI1_PWDN | GPIO33 | | CCI_ASYNC0 | |
| J71-57 | CSI1_RESET | GPIO28 | CAM1_RST | | |
| J70-70 | DSI0_RESET | GPIO25 | DSI_RST | GP_PDM_0B | |
| J70-72 | DSI0_ENABLE | GPIO32 | | CCI_TIMER1 | GP_CLK1 |
| J70-76 | BACKLIGHT_ENABLE | GPIO98 | LCD_BL_EN | | GP_PDM_2A |
| J71-5 | HDMI_INT | GPIO31 | GP_CLK0 | CCI_TIMER0 | |
| J70-95 | SD2_CARDDETECT_N | GPIO38 | SD_CARD_DET | CCI_TIMER2 | |
| J70-97 | SD2_WRITEPROTECT | GPIO69 | | SPI3_CS3 | |
| J71-6 | KYPD_SNS0 | GPIO107 | KYPD_SNS0 | | |
| J71-8 | KYPD_SNS1 | GPIO108 | KYPD_SNS1 | | |
| J71-10 | KYPD_SNS2 | GPIO109 | KYPD_SNS2 | | |
| J71-12 | USR_LED2 | GPIO120 | | SPI3_CS1 | |
| J70-25 | USB_OTG_VBUS Signal connected through 100k/47K resistor divider | GPIO121 | | SPI2_CS1 | |
| J71-62 | GPIO78 | GPIO78 | | | |
| J71-64 | GPIO79 | GPIO79 | | | |
| J71-66 | GPIO95 | GPIO95 | | | |
| J71-68 | GPIO99 | GPIO99 | | | |
| J71-70 | GPIO100 | GPIO100 | | | |
| J71-72 | GPIO101 | GPIO101 | | | |
| J71-74 | GPIO102 | GPIO102 | | | |
| J71-76 | GPIO103 | GPIO103 | SSBI_WTR0_RX | | |
| J71-82 | GPIO59 | GPIO59 | UIM1_RST | | |
| J71-84 | GPIO60 | GPIO60 | UIM1_PRESENT | | |
| J71-86 | GPIO58 | GPIO58 | UIM1_CLK | | |
| J71-88 | GPIO57 | GPIO57 | UIM1_DATA | | |
| J71-90 | GPIO61 | GPIO61 | UIM_BATT_ALARM | | |
| J71-92 | GPIO62 | GPIO62 | SMB_INT | | |
| J71-94 | GPIO105 | GPIO105 | SSBI_WTR1_RX | | |
| J71-96 | GPIO106 | GPIO106 | SSBI_WTR1_TX | | |
| J71-98 | GPIO96 | GPIO96 | EXT_GNSS_LNA_EN | | |

## 1.3 Electrical Pin-Information

PI: Power Input
PO: Power Output
CO: Charger Output

AI: Analog Input
AO: Analog Output
ADI: Analog Differential Input
ADO: Analog Differential Output
ADIO: Analog Differential Input/Output

DI: Digital Input
DO: Digital Output
DIO: Digital Input/Output

PD: Pull-Down (PDp: Pull-Down, Pull-behavior can be changed by software)
PU: Pull-Up (PUp: Pull-Up, Pull-behavior can be changed by software)

| PIN | Name | Type | Voltage | Connected to |
|---|---|---|---|---|
| J70-1 | VBAT | PI,CO | Typ. 3.7V | PM8916 |
| J70-2 | VBAT | | | |
| J70-5 | VBAT | | | |
| J70-7 | VBAT | | | |
| J70-9 | BAT_THERM | AI | | PM8916 |
| J70-11 | VBAT_COIN | PI,CO | Typ. 3.0V | PM8916 |
| J70-13 | GND | | | |
| J70-15 | GND | | | |
| J70-17 | USB_VBUS | PI | Typ. 5V | PM8916 |
| J70-19 | USB_VBUS | | | |
| J70-21 | USB_VBUS | | | |
| J70-23 | USB_VBUS | | | |
| J70-25 | USB_OTG_VBUS | DI | (+1V8) connected through Resistor-Divider 1/3.1 | APQ8016 |
| J70-27 | USB_OTG_DM | ADIO | | |
| J70-29 | USB_OTG_DP | ADIO | | |
| J70-31 | USB_OTG_ID | | | APQ8016 |
| J70-33 | GND | | | |
| J70-35 | GND_CFILT | Analog Audio Ground | | PM8916 |
| J70-37 | MIC2 | AI | | PM8916 |
| J70-39 | MIC_BIAS2 | AO | | PM8916 |
| J70-41 | HEADPHONE_L | AO | | PM8916 |
| J70-43 | HEADPHONE_R | AO | | PM8916 |
| J70-45 | HEADPHONE_REF | AI | | PM8916 |
| J70-47 | HEADSET_DETECT | AI | | PM8916 |
| J70-49 | MIC1 | AI | | PM8916 |
| J70-51 | MIC_BIAS1 | AO | | PM8916 |
| J70-53 | FM_ANTENNA | AI | | WCN3620 |
| J70-55 | MIC3 | AI | | PM8916 |
| J70-57 | SPEAKER_P | AO | | PM8916 |
| J70-59 | SPEAKER_N | AO | | PM8916 |

| PIN | Name | Type | Voltage | Connected to |
|---|---|---|---|---|
| J70-61 | P1_TXD_MOSI | DIO,PDp | +1V8_IO | APQ8016 |
| J70-63 | P1_RXD_MISO | DIO,PDp | +1V8_IO | APQ8016 |
| J70-65 | P1_RTS_CLK_SCL | DIO,PDp | +1V8_IO | APQ8016 |
| J70-67 | P1_CTS_CS_SDA | DIO,PDp | +1V8_IO | APQ8016 |
| J70-69 | P2_TXD_MOSI | DIO,PDp | +1V8_IO | APQ8016 |
| J70-71 | P2_RXD_MISO | DIO,PDp | +1V8_IO | APQ8016 |
| J70-73 | P2_RTS_CLK_SCL | DIO,PDp | +1V8_IO | APQ8016 |
| J70-75 | P2_CTS_CS_SDA | DIO,PDp | +1V8_IO | APQ8016 |
| J70-77 | GND | | | |
| J70-79 | VDD_SDCARD_PWR | PO | 1.8V/3.3V | PM8916 |
| J70-81 | VDD_SDCARD_IO | PO | 1.8V/3.3V | PM8916 |
| J70-83 | SD2_CMD | DIO,NPp | VDD_SDCARD_IO | APQ8016 |
| J70-85 | SD2_CLK | DIO,PDp | VDD_SDCARD_IO | APQ8016 |
| J70-87 | SD2_DAT0 | DIO,PDp | VDD_SDCARD_IO | APQ8016 |
| J70-89 | SD2_DAT1 | DIO,PDp | VDD_SDCARD_IO | APQ8016 |
| J70-91 | SD2_DAT2 | DIO,PDp | VDD_SDCARD_IO | APQ8016 |
| J70-93 | SD2_DAT3 | DIO,PDp | VDD_SDCARD_IO | APQ8016 |
| J70-95 | SD2_CARDDETECT_N | DIO,PDp | +1V8_IO | APQ8016 |
| J70-97 | SD2_WRITEPROTECT | DIO,PDp | +1V8_IO | APQ8016 |
| J70-99 | GND | | | |
| J70-2 | VBAT | PI,CO | Typ. 3.7V | PM8916 |
| J70-4 | VBAT | | | |
| J70-6 | VBAT | | | |
| J70-8 | VBAT | | | |
| J70-10 | BAT_SENSE | AI | | PM8916 |
| J70-12 | BAT_ID | AI | | PM8916 |
| J70-14 | GND | | | |
| J70-16 | GND | | | |
| J70-18 | USB_VBUS | PI,CO | Typ. 5V | PM8916 |
| J70-20 | USB_VBUS | | | |
| J70-22 | USB_VBUS | | | |
| J70-24 | USB_VBUS | | | |
| J70-26 | USB_VBUS | | | |
| J70-28 | PHONE_ON_N | DI,PU | Int.Voltage, Only switch to GND by external circuit. | PM8916 |
| J70-30 | RESET_IN_N | DI,PU | | PM8916 |
| J70-32 | RESET_OUT_N | DO | +1V8_IO | APQ8016 |
| J70-34 | GND | | | |
| J70-36 | GND | | | |
| J70-38 | JTAG_MODE | DI,PD | +1V8_IO | APQ8016 |
| J70-40 | FORCE_USB_BOOT | DI,PD | +1V8_IO | APQ8016 |
| J70-42 | +3V3 | PO | 3.3V | PM8916 |
| J70-44 | +3V3 | | | |
| J70-46 | +1V8_MIPI | PO | 1.8V | PM8916 |
| J70-48 | +1V8_MIPI | | | |
| J70-50 | +1V8_EXT | PO | 1.8V | PM8916 |

| PIN | Name | Type | Voltage | Connected to |
|---|---|---|---|---|
| J70-52 | +1V8_IO | PO | 1.8V | PM8916 |
| J70-54 | P3_MOSI | DIO,PDp | +1V8_IO | APQ8016 |
| J70-56 | P3_MISO | DIO,PDp | +1V8_IO | APQ8016 |
| J70-58 | P3_CLK_SCL | DIO,PDp | +1V8_IO | APQ8016 |
| J70-60 | P3_CS_SDA | DIO,PDp | +1V8_IO | APQ8016 |
| J70-62 | P4_MOSI | DIO,PDp | +1V8_IO | APQ8016 |
| J70-64 | P4_MISO | DIO,PDp | +1V8_IO | APQ8016 |
| J70-66 | P4_CLK_SCL | DIO,PDp | +1V8_IO | APQ8016 |
| J70-68 | P4_CS_SDA | DIO,PDp | +1V8_IO | APQ8016 |
| J70-70 | DSI0_RESET | DIO,PDp | +1V8_IO | APQ8016 |
| J70-72 | DSI0_ENABLE | DIO,PDp | +1V8_IO | APQ8016 |
| J70-74 | BACKLIGHT_PWM | DIO | V_M | PM8916 |
| J70-76 | BACKLIGHT_ENABLE | DIO,PDp | +1V8_IO | APQ8016 |
| J70-78 | GND | | | |
| J70-80 | DSI0_DAT0_N / LVDS_TXN0 | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-82 | DSI0_DAT0_P / LVDS_TXP0 | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-84 | DSI0_DAT1_N / LVDS_TXN1 | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-86 | DSI0_DAT1_P / LVDS_TXP1 | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-88 | DSI0_DAT2_N / LVDS_TXN2 | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-90 | DSI0_DAT2_P / LVDS_TXP2 | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-92 | DSI0_DAT3_N / LVDS_TXN3 | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-94 | DSI0_DAT3_P / LVDS_TXP3 | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-96 | DSI0_CLK_N / LVDS_CLKN | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-98 | DSI0_CLK_P / LVDS_CLKP | ADO | +1V2 (MIPI) +1V8_MIPI | APQ8016 / SN65DSI83 |
| J70-100 | GND | | | |
| J71-1 | BOOT_CONFIG_1 | DI,PD | +1V8_IO | APQ8016 |
| J71-3 | BBCLK2 | DO | +1V8 | PM8916 |
| J71-5 | HDMI_INT | DIO,PDp | +1V8_IO | APQ8016 |
| J71-7 | P5_MOSI | DIO,PDp | +1V8_IO | APQ8016 |
| J71-9 | P5_MISO | DIO,PDp | +1V8_IO | APQ8016 |
| J71-11 | P5_CLK_SCL | DIO,PDp | +1V8_IO | APQ8016 |
| J71-13 | P5_CS_SDA | DIO,PDp | +1V8_IO | APQ8016 |
| J71-15 | P6_MOSI | DIO,PDp | +1V8_IO | APQ8016 |
| J71-17 | P6_MISO | DIO,PDp | +1V8_IO | APQ8016 |
| J71-19 | P6_CLK_SCL | DIO,PDp | +1V8_IO | APQ8016 |
| J71-21 | P6_CS_SDA | DIO,PDp | +1V8_IO | APQ8016 |
| J71-23 | I2S1_DAT0 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-25 | I2S1_DAT1 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-27 | I2S1_SCK | DIO,PDp | +1V8_IO | APQ8016 |
| J71-29 | I2S1_MCLK | DIO,PDp | +1V8_IO | APQ8016 |
| J71-31 | I2S1_WS | DIO,PDp | +1V8_IO | APQ8016 |

| PIN | Name | Type | Voltage | Connected to |
|---|---|---|---|---|
| J71-33 | I2S2_DAT0 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-35 | I2S2_DAT1 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-37 | I2S2_SCK | DIO,PDp | +1V8_IO | APQ8016 |
| J71-39 | I2S2_WS | DIO,PDp | +1V8_IO | APQ8016 |
| J71-41 | GND | | | |
| J71-43 | CSI1_CLK_N | ADI | +1V2 (MIPI) | APQ8016 |
| J71-45 | CSI1_CLK_P | ADI | +1V2 (MIPI) | APQ8016 |
| J71-47 | CSI1_DAT0_N | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-49 | CSI1_DAT0_P | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-51 | CSI1_DAT1_N | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-53 | CSI1_DAT1_P | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-55 | GND | | | |
| J71-57 | CSI1_RESET | DIO,PDp | +1V8_IO | APQ8016 |
| J71-59 | CSI1_PWDN | DIO,PDp | +1V8_IO | APQ8016 |
| J71-61 | CSI1_MCLK | DIO,PDp | +1V8_IO | APQ8016 |
| J71-63 | CAM_TORCH | DIO,PDp | +1V8_IO | APQ8016 |
| J71-65 | CAM_FLASH | DIO,PDp | +1V8_IO | APQ8016 |
| J71-67 | CAM_I2C_SCL | DIO,PDp | +1V8_IO | APQ8016 |
| J71-69 | CAM_I2C_SDA | DIO,PDp | +1V8_IO | APQ8016 |
| J71-71 | CSI0_RESET | DIO,PDp | +1V8_IO | APQ8016 |
| J71-73 | CSI0_PWDN | DIO,PDp | +1V8_IO | APQ8016 |
| J71-75 | CSI0_MCLK | DIO,PDp | +1V8_IO | APQ8016 |
| J71-77 | GND | | | |
| J71-79 | CSI0_CLK_N | ADI | +1V2 (MIPI) | APQ8016 |
| J71-81 | CSI0_CLK_P | ADI | +1V2 (MIPI) | APQ8016 |
| J71-83 | CSI0_DAT0_N | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-85 | CSI0_DAT0_P | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-87 | CSI0_DAT1_N | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-89 | CSI0_DAT1_P | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-91 | CSI0_DAT2_N | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-93 | CSI0_DAT2_P | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-95 | CSI0_DAT3_N | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-97 | CSI0_DAT3_P | ADIO | +1V2 (MIPI) | APQ8016 |
| J71-99 | GND | | | |
| J71-2 | WLAN_LED | DIO | V_M | PM8916 |
| J71-4 | BT_LED | DIO | V_M | PM8916 |
| J71-6 | KYPD_SNS0 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-8 | KYPD_SNS1 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-10 | KYPD_SNS2 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-12 | USR_LED2 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-14 | USR_LED3 | DIO | V_G | PM8916 |
| J71-16 | USR_LED4 | DIO | V_G | PM8916 |
| J71-18 | USB_HUB_RESET_N | DO | V_G | PM8916 |
| J71-20 | USB_SW_SEL | DO | V_G | PM8916 |
| J71-42 | GND | | | |
| J71-56 | GND | | | |
| J71-62 | GPIO78 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-64 | GPIO79 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-66 | GPIO95 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-68 | GPIO99 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-70 | GPIO100 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-72 | GPIO101 | DIO,PDp | +1V8_IO | APQ8016 |

| PIN | Name | Type | Voltage | Connected to |
|---|---|---|---|---|
| J71-74 | GPIO102 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-76 | GPIO103 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-78 | GND | | | |
| J71-82 | GPIO59 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-84 | GPIO60 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-86 | GPIO58 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-88 | GPIO57 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-90 | GPIO61 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-92 | GPIO62 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-94 | GPIO105 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-96 | GPIO106 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-98 | GPIO96 | DIO,PDp | +1V8_IO | APQ8016 |
| J71-100 | GND | | | |

**Notes on V_M and V_G:**
The supply of the GPIO and MPP pins of the PMX8916 can be configured by software.
See GPIOx_DIG_VIN_CTL and MPPx_DIG_VIN_CTL in PM8916 Hardware Register Description.

0 VBAT
1 VBAT
2 VREG_L2 ( +1V2)
3 VREG_L5 ( +1V8_IO)

# 2. Interfaces

This chapter includes a short description of all interfaces of the Myon I.
Please consult the processor datasheet for detailed information.

## 2.1 Power Supply

There are two main power supply scenarios. Battery power supply and external power supply.

| Name | Description |
|---|---|
| VBAT | Main power input.<br>Battery node; input during battery operation, output during charging. |
| BAT_THERM | Main battery thermistor analog input. |
| BAT_SENSE | Main battery voltage sense point. |
| BAT_ID | Main battery ID analog input |
| VBAT_COIN | Coin-Cell sense input or charge output.<br>Leave unconnected if not used. |
| USB_VBUS | Input power for charger. Typically from USB-connector. |
| +3V3 | +3.3V power output (max. 450mA) |
| +1V8_MIPI | +1.8V power output (max. <150mA)<br>Note that this regulator also supplies on-board peripherals. So the current available for use by the baseboard is less than 150mA. |
| +1V8_EXT | +1.8V power output (max. 110mA) |
| +1V8_IO | +1.8V power output (max. <200mA)<br>Note that this regulator also supplies the IO-voltage of on-board peripherals. So the current available for use by the baseboard is less than 200mA. If possible the IO-voltage of the baseboards peripherals should be connected to this supply. |

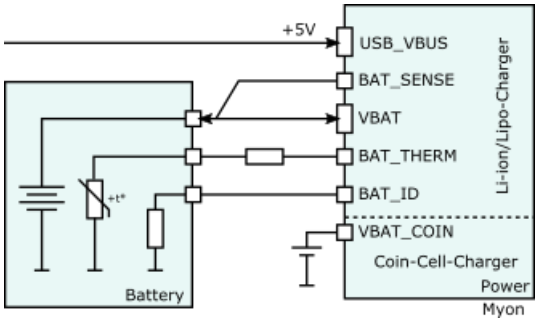
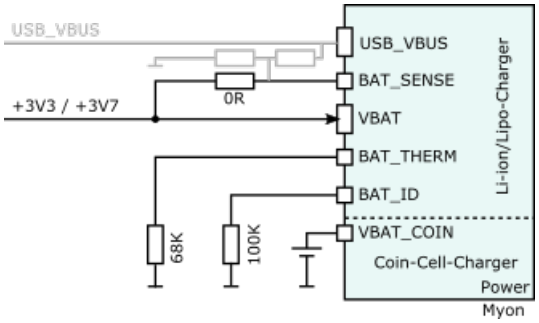



Figure 2-1-1 Application Diagram Battery Power Supply




The circuit will depend on operating system driver requirements. (Sensing of battery and USB detection)
If VBAT is set to +3.3V, you need to remove the 68K pull-down on BAT_THERM or the software may stop booting.
If a USB-cable is plugged (USB_VBUS=+5V), you might need to supply +3.7V to BAT_SENSE or the software may stop booting the OS. The processor Boot-ROM code ignores BAT_SENSE and thus in that case updating the OS through USB is still possible.
The simplest option would be to supply VBAT with 3.7V.

Figure 2-1-2 Application Diagram External Power Supply

## 2.2 Control-Signals

| Name | Description |
|---|---|
| PHONE_ON_N | Connect to power-on/off button. The signal got a pull-up to an internal voltage. Only pull signal to ground by external circuit. |
| RESET_IN_N | Negated reset input. 0: reset device, 1: normal operation. |
| RESET_OUT_N | Negated reset output. 0: device in reset, 1: normal operation. |
| JTAG_MODE | Leave unconnected for JTAG Native Mode / normal operation.<br>Connect to +1V8_IO for JTAG Boundary Scan testing. |
| FORCE_USB_BOOT | Pull to +1V8_IO to force boot through a USB connection with a PC. |
| USB_OTG_VBUS | Connect to VBUS(+5V) of USB-OTG-connector. Used by software to detect if USB-Slave cable got connected. |
| BOOT_CONFIG_1 | Not connected (Gnd): Boot from eMMC (eMMC → SD-Card → USB)<br>Pull to +1V8_IO: Boot from SD-Card ( SD-Card → eMMC → USB) |

Figure 2-2-1 Application Diagram PHONE_ON and RESET_IN usage.

## 2.3 IO-Ports 1–6

| Name | Description |
|---|---|
| P1_TXD_MOSI | GPIO0; UART1_TXD or SPI1_MOSI output |
| P1_RXD_MISO | GPIO1; UART1_RXD or SPI1_MISO input |
| P1_RTS_CLK_SCL | GPIO3; UART1_RTS, SPI1_CLK or I2C1_SCL output |
| P1_CTS_CS_SDA | GPIO2; I2C1_SDA; UART1_CTS input; SPI1_CS output |
| P2_TXD_MOSI | GPIO4; UART2_TXD or SPI2_MOSI output |
| P2_RXD_MISO | GPIO5; UART2_RXD or SPI2_MISO input |
| P2_RTS_CLK_SCL | GPIO7; UART2_RTS, SPI2_CLK or I2C2_SCL output |
| P2_CTS_CS_SDA | GPIO6; I2C2_SDA; UART2_CTS input; SPI2_CS output |
| P3_MOSI | GPIO8; SPI3_MOSI output |
| P3_MISO | GPIO9; SPI3_MISO input |
| P3_CLK_SCL | GPIO11; SPI3_CLK or I2C3_SCL output |
| P3_CS_SDA | GPIO10; SPI3_CS output; I2C3_SDA |
| P4_MOSI | GPIO12; SPI4_MOSI output |
| P4_MISO | GPIO13; SPI4_MISO input |
| P4_CLK_SCL | GPIO15; SPI4_CLK or I2C4_SCL output |
| P4_CS_SDA | GPIO14; SPI4_CS output; I2C4_SDA |
| P5_MOSI | GPIO16; SPI5_MOSI output |
| P5_MISO | GPIO17; SPI5_MISO input |
| P5_CLK_SCL | GPIO19; SPI5_CLK or I2C5_SCL output |
| P5_CS_SDA | GPIO18; SPI5_CS output; I2C5_SDA |
| P6_MOSI | GPIO20; SPI6_MOSI output |
| P6_MISO | GPIO21; SPI6_MISO input |
| P6_CLK_SCL | GPIO23; SPI6_CLK or I2C6_SCL output |
| P6_CS_SDA | GPIO22; SPI6_CS output; I2C6_SDA |

**Possible Muxing Sheme:**

| 4-pin UART | I2C, GPIO | I2C, 2-pin UART | 4-pin SPI | GPIO |
|---|---|---|---|---|
| Px_TXD | Px_GPIOxx | Px_TXD | Px_MOSI | Px_GPIOxx |
| Px_RXD | Px_GPIOxx | Px_RXD | Px_MISO | Px_GPIOxx |
| Px_RTS | Px_SCL | Px_SCL | Px_CLK | Px_GPIOxx |
| Px_CTS | Px_SDA | Px_SDA | Px_CS | Px_GPIOxx |

### 2.3.1 GPIO

GPIO pins may be configured as input or outputs and with pull-up, pull-down, keeper or no pull – behavior. The pins have a programmable drive-current of 2..16mA in 2mA steps.

### 2.3.2 UART

Baudrate: 75 to 115.200 bps and 4Mbps
Dara-Bits: 5 to 8 bits
Stop-Bits: 0.5, 1, 2
Parity: None, Event, Odd, Space
Features: Hardware-flow-control (RTS,CTS)

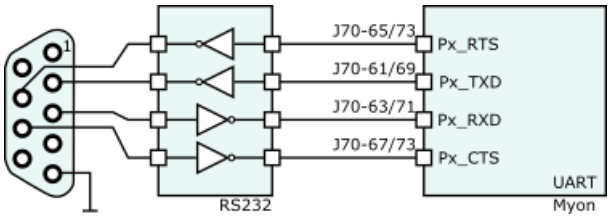



Figure 2-3-2-1: Application Diagram RS232

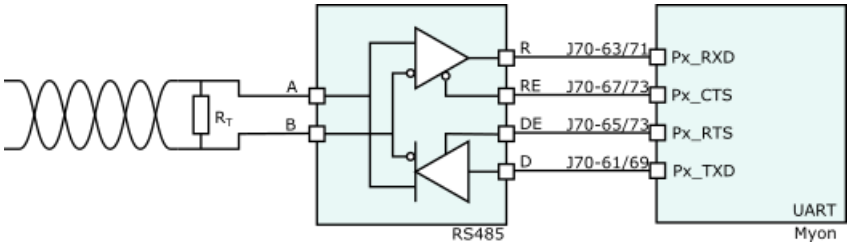



Figure 2-3-2-2: Application Diagram RS485

### 2.3.3 SPI

The serial peripheral interface is a programmable synchronous serial port, which may be used to connect to a multiple of different peripherals.
The IO-Ports only define a 4pin SPI with one chip-select. Extra SPI-chip-selects can be found on other GPIOs ( see "1.2 Pin-Mux Information").

Speed: up to 50Mhz
Features: Master only.

### 2.3.4 I2C

Speed: up to 3.7Mhz
Features: Master only.
$I^2C$ Specification Version 5.0, Oktober 2012
Multi-Master, 10bit addressing or HS-mode is not supported.

## 2.4 I2S-IO-Ports

The Inter-IC sound interface is used to connect to audio codecs.
The APQ8016 supports a multichannel $I^2S$. The multichannel $I^2S$ adds one channel to the standard $I^2S$.

| Name | Description |
|---|---|
| I2S1_DAT0 | First I2S-port: serial data channel 0 |
| I2S1_DAT1 | First I2S-port: serial data channel 1 |
| I2S1_SCK | First I2S-port: bit clock |
| I2S1_WS | First I2S-port: word select (L/R) |
| I2S1_MCLK | First I2S-port: master clock output |
| I2S2_DAT0 | Second I2S-port: serial data channel 0 |
| I2S2_DAT1 | Second I2S-port: serial data channel 1 |
| I2S2_SCK | Second I2S-port: bit clock |
| I2S2_WS | Second I2S-port: word select (L/R) |

Speed: up to 12.288MHz.
Features: Philips $I^2S$ Bus Specification June 5, 1996.
$I^2S$ format: data is transmitted on falling edge and latched at rising edge of the clock.
16, 23 and 32bit modes supported.

## 2.5 SD-Card

The SD-Card Interface may be used to connect a SD-Card, eMMC or SDIO-hardware to the Myon board.

| Name | Description |
|---|---|
| VDD_SDCARD_PWR | Power supply output for the attached SD/SDIO-peripheral (1.8V – 3.3V) |
| VDD_SDCARD_IO | IO-Voltage for SD2_xxx signals ( 1.8V / 2.95V) |
| SD2_CMD | SD-card command output |
| SD2_CLK | SD-card clk output |
| SD2_DAT0 | SD-card data bit 0 |
| SD2_DAT1 | SD-card data bit 1 |
| SD2_DAT2 | SD-card data bit 2 |
| SD2_DAT3 | SD-card data bit 3 |
| SD2_CARDDETECT_N | SD-card detect: 0: card inserted, 1: card removed |
| SD2_WRITEPROTECT | SD-card write-protect |

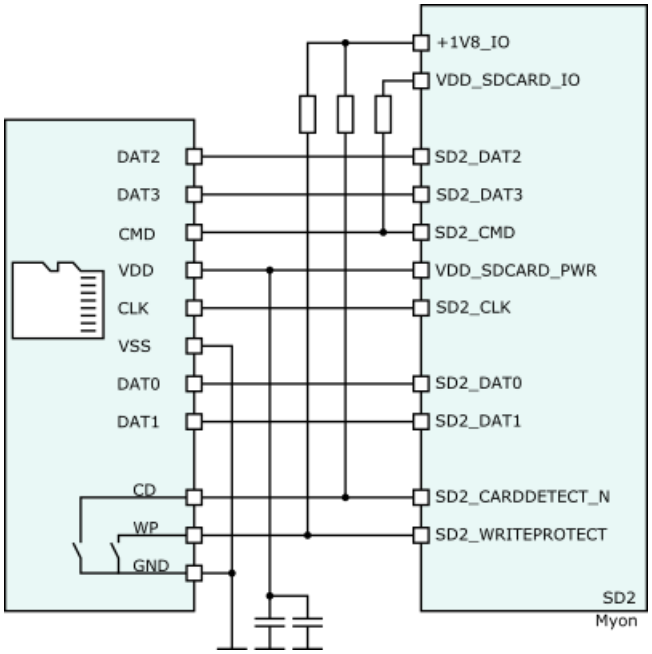



Figure 2-5-1: Application Diagram SD-Card-Socket

## 2.6 USB

The Myon I got one high-speed USB 2.0 OTG port which may work as host or as slave.

| Name | Description |
|---|---|
| USB_OTG_VBUS | Connect to VBUS (+5) of USB-Slave or USB-OTG port. This is a simple GPIO, which is used to detect if the port should work as slave. |
| USB_OTG_DM | USB HS data minus |
| USB_OTG_DP | USB HS data plus |
| USB_OTG_ID | USB OTG ID pin. |

Speed: 480Mbps
Features: USB2.0 high-speed.

## 2.7 Display

The Myon I has two different mounting options for the display-port pins:

- MIPI signals (DSI0_xxx)
- LVDS signals ( LVDS_xxx)

| Name | Description |
|---|---|
| DSI0_DAT0_N / LVDS_TXN0 | Display data lane 0 – negative |
| DSI0_DAT0_P / LVDS_TXP0 | Display data lane 0 – positive |
| DSI0_DAT1_N / LVDS_TXN1 | Display data lane 1 – negative |
| DSI0_DAT1_P / LVDS_TXP1 | Display data lane 1 – positive |
| DSI0_DAT2_N / LVDS_TXN2 | Display data lane 2 - negative |
| DSI0_DAT2_P / LVDS_TXP2 | Display data lane 2 - positive |
| DSI0_DAT3_N / LVDS_TXN3 | Display data lane 3 – negative |
| DSI0_DAT3_P / LVDS_TXP3 | Display data lane 3 – positive |
| DSI0_CLK_N / LVDS_CLKN | Display data clock – negative |
| DSI0_CLK_P / LVDS_CLKP | Display data clock – positive |
| DSI0_RESET | Display reset (output) |
| DSI0_ENABLE | Display enable (output) |
| BACKLIGHT_PWM | Backlight PWM (output) |
| BACKLIGHT_ENABLE | Backlight enable (output) |
| HDMI_INT | HDMI interrupt input |

Features: HD (1280 x 720) 60 fps; 16/18/24 bpp RGB
MIPI DSI 4-lane
Wifi display – 720p 30fps / 1080p 30fps

## 2.8 Camera

The Myon I got two MIPI camera interfaces.
CSI0 is the main-camera interface.
CAM_xxx signals are shared by both cameras.

| Name | Description |
|---|---|
| CSI0_CLK_N | Main camera clock input – negative |
| CSI0_CLK_P | Main camera clock input – positive |
| CSI0_DAT0_N | Main camera data lane 0 – negative |
| CSI0_DAT0_P | Main camera data lane 0 – positive |
| CSI0_DAT1_N | Main camera data lane 1 – negative |
| CSI0_DAT1_P | Main camera data lane 1 – positive |
| CSI0_DAT2_N | Main camera data lane 2 – negative |
| CSI0_DAT2_P | Main camera data lane 2 – positive |
| CSI0_DAT3_N | Main camera data lane 3 – negative |
| CSI0_DAT3_P | Main camera data lane 3 – positive |
| CSI0_RESET | Main camera reset |
| CSI0_PWDN | Main camera power-down / enable |
| CSI0_MCLK | Main camera master clock output |
| CSI1_CLK_N | Aux camera clock input – negative |
| CSI1_CLK_P | Aux camera clock input – positive |
| CSI1_DAT0_N | Aux camera data lane 0 – negative |
| CSI1_DAT0_P | Aux camera data lane 0 – positive |
| CSI1_DAT1_N | Aux camera data lane 1 – negative |
| CSI1_DAT1_P | Aux camera data lane 1 – positive |
| CSI1_RESET | Aux camera reset |
| CSI1_PWDN | Aux camera power-down / enable |
| CSI1_MCLK | Aux camera master clock output |
| CAM_TORCH | Camera torch on / light on |
| CAM_FLASH | Camera flash |
| CAM_I2C_SCL | Camera I2C clock |
| CAM_I2C_SDA | Camera I2C data |

CSI0 Features: Up to 13 MPixel sensors
4-lane; 1.5 Gbps per lane
Supports CMOS and CCD sensors

CSI1 Features: Up to 8 MPixel sensors
2-lane; 1.5 Gbps per lane

## 2.9 Wireless

| Name | Description |
|---|---|
| WLAN_LED | WLAN active LED |
| BT_LED | Bluetooth active LED |
| FM_ANTENNA | FM-radio-antenna. 76 to 108 MHz with 50kHz channel spacing. |

GPS functionality: If this function is required, please contact Keith & Koep.

## 2.10 Audio

| Name | Description |
|---|---|
| GND_CFILT | Analog ground for audio |
| MIC1 | Main mic input |
| MIC_BIAS1 | Microphone bias #1 output |
| MIC2 | Headset mic input |
| MIC_BIAS2 | Microphone bias #2 output |
| MIC3 | Second mic input |
| HEADPHONE_L | Headphone left channel output |
| HEADPHONE_R | Headphone right channel output |
| HEADPHONE_REF | Headphone ground sensing input |
| HEADSET_DETECT | Headset detect input |
| SPEAKER_P | Class-D speaker amp + output |
| SPEAKER_N | Class-D speaker amp - output |

## 2.11 JTAG

| Name | Description |
|---|---|
| JTAG_TMS | JTAG mode-select input |
| JTAG_TRST_N | JTAG reset |
| JTAG_TCK | JTAG clock input |
| JTAG_TDO | JTAG data output |
| JTAG_TDI | JTAG data input |
| JTAG_SRST_N | JTAG reset for debug |

## 2.12 Miscellaneous Signals

| Name | Description |
|---|---|
| BBCLK2 | Baseband XO output 2 of PM8916 PMIC (19.2MHz) |
| KYPD_SNS0 | Keypad sense bit 0 |
| KYPD_SNS1 | Keypad sense bit 1 |
| KYPD_SNS2 | Keypad sense bit 2 |
| USR_LED2 | User LED |
| USR_LED3 | User LED |
| USR_LED4 | User LED |
| USB_HUB_RESET_N | GPIO3 of PM8916 PMIC. 'Default' function is USB hub reset output |
| USB_SW_SEL | GPIO4 of PM8916 PMIC. 'Default' function is USB switch sel output. 0: USB in device mode; 1: USB in host mode |

## 2.13 Realtime Clock

If it is needed, it is recommended to use an external Realtime-Clock i.e. EPSON RTC-8564JE to keep the time during low-power or power-off -modes.

# 3. Specifications

## 3.1 Absolute Maximum Ratings

Absolute maximum ratings reflect conditions that the module may be exposed outside of the operating limits, without experiencing immediate functional failure. Functional operation is only expected during the conditions indicated under "Recommended Operating Conditions". Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the module. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

| Name | Pin | Min | | Max | Unit |
|---|---|---|---|---|---|
| **Supply Voltage** | VBAT | -0.5 | | 6 | V |
| | USB_VBUS | -0.5 | | 16 | V |
| **Storage Temperature** | $T_{Storage}$ | -50 | | 100 | °C |

## 3.2 ESD Ratings

| Name | Description | Max | Unit |
|---|---|---|---|
| **$V_{(ESD)}$ Electrostatic discharge** | Human body model (HBM) | ±2000 | V |
| | Charged-device model (CDM) | ±500 | |

## 3.3 Recommended Operating Conditions

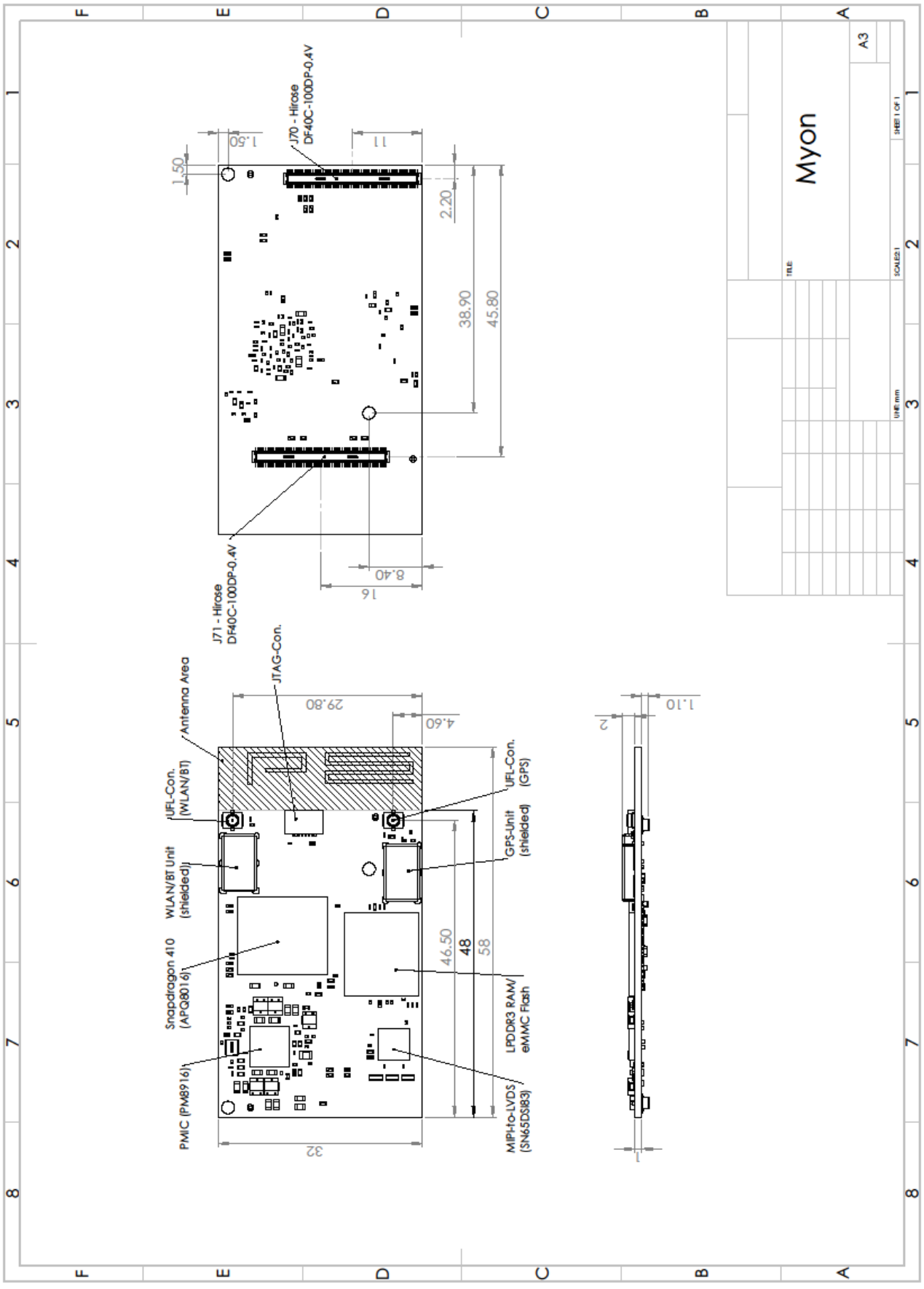
| Name | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Supply Voltage** | VBAT | 3.0 | 3.6 | 4.5 | V |
| | USB_VBUS | 4.35 | - | 6.2 | V |
| | VBAT_COIN | 2.0 | 3.0 | 3.25 | V |
| **Supply current (typ.)**<br>Measured on ConXM with HDMI-output and Win10 IOT / Linux.<br>Power consumption dramatically depends on the usage scenario.<br>This includes things like if the processors operating point (frequency) can be set to a lower level; if the GPU can be used by an application; the selected display-resolution or if the module supplies external peripherals i.e. a speaker or if the PMIC charges a battery.<br><br>**We recommend to use a min. 2A voltage-regulator to supply the module.** | VBAT @ 3.3V | | | | mA |
| | Idle | | 220 | | mA |
| | Using/Running | 300 | | 800 | mA |
| | Typ. Peak Currents when running. | 1 | | 1.5 | A |
| **Operating temperature** | $T_{Case}$ | -25 | +25 | +85 | °C |
| | $T_{Ambient}$ | -25 | +25 | +60 | |

## 3.4 Electrical Characteristics

| | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IL\_1V8}$ | Low-level input voltage | - | 0.35 * (+1V8_IO) | V |
| $V_{IH\_1V8}$ | High-level input voltage | 0.65 * (+1V8_IO) | - | V |
| $V_{OH\_1V8}$ | High-level output voltage | (+1V8_IO) – 0.45 | - | V |
| $V_{IH\_1V8}$ | Low-level output voltage | - | 0.45 | V |
| $R_{P\_1V8}$ | Pull-Resistance | 55 | 390 | kΩ |
| $R_{K\_1V8}$ | Keeper-Resistance | 30 | 150 | kΩ |

## 3.5 Mechanical Specification

We strongly recommend the use of plastic screws (for example M2.0x8mm, DIN 84 / ISO 1207 PA 6.6) as mounting parts to prevent possible short-circuits.



# 4.0 Ordercodes for Myon I

| Order Code 00... | Myon I (without image) |
|---|---|
| 40 024.MI00. H00S00 | Myon I/SD410/R1G/EMMC8G/BW/MIPI/RoHS (Snapdragon 410, 1,2 GHz, 1 GB RAM, 8 GB eMMC, WLAN, Bluetooth, MIPI) |
| 40 024.LV00. H00S00 | Myon I/SD410/R1G/EMMC8G/BW/LVDS/RoHS (Snapdragon 410, 1,2 GHz, 1 GB RAM, 8 GB eMMC, WLAN, Bluetooth, LVDS) |
| 40 024.MK00. H00S00 | Myon I/SD410/R1G/EMMC8G/WB/MIPI/noANT/RoHS (Snapdragon 410, 1,2 GHz, 1 GB RAM, 8 GB eMMC, WLAN, Bluetooth, MIPI, no antenna) |
| 40 024.LK00. H00S00 | Myon I/SD410/R1G/EMMC8G/WB/LVDS/noANT/RoHS (Snapdragon 410, 1,2 GHz, 1 GB RAM, 8 GB eMMC, WLAN, Bluetooth, LVDS, no antenna) |
| 40 014.MK00. H00S00 | Myon I/SD410/R1G/EMMC8G/woWB/woGPS/MIPI/RoHS (Snapdragon 410, 1,2 GHz, 1 GB RAM, 8 GB eMMC, MIPI, without WLAN, without Bluetooth, without GPS) |
| 40 014.LK00. H00S00 | Myon I/SD410/R1G/EMMC8G/woWB/woGPS/LVDS/RoHS (Snapdragon 410, 1,2 GHz, 1 GB RAM, 8 GB eMMC, LVDS, without WLAN, without Bluetooth, without GPS) |

# 5. Important Notice

# 6. Document History

| Rev. | Date | Author | Changes |
|---|---|---|---|
| 0.9 | 28.01.2016 | SH | Initial Version. |
| 1.0 | 18.02.2017 | SH | Minor changes |
| 1.1 | 08.06.2017 | JP | Pictures added<br>Mounting recommendations |
| 1.2 | 13.07.2017 | SH | Add power-consumption details. |
| 1.3 | 04.09.2017 | CT | Pictures changed/added<br>Layout edited<br>Ordercodes added |
| 1.4 | 20.10.2017 | SH | Added GPIO pins J71.16, J71.62-J71.98 to datasheet. |
| 1.5 | 19.04.2018 | SH | Added Figure 2-1-2 Application Diagram External Power Supply |
| 1.6 | 14.02.2019 | SH | Added notes about supply voltage of PM8916 GPIO and MPP pins beeing configurable by software. (1.3 Electrical Pin Information) |
| 1.7 | 10.04.2019 | SH | Added 2.13 Realtime-Clock |
| 1.8 | 20.05.2019 | CT | Added Myon pictures, improved graphic design<br>Added order codes |
| 1.9 | 03.09.2019 | CT | Added note to GPS functionality (page 20) |